CTC CPU PRELIMINARY DESCRIPTION

THE CPU IS AN 8 BIT PARALLEL CENTRAL PROCESSOR UNIT FOR A COMPUTER SYSTEM. IT CAN BE INTERFACED WITH VARIOUS MEMORIES HAVING CAPACITIES UP TO 16K BYTES.

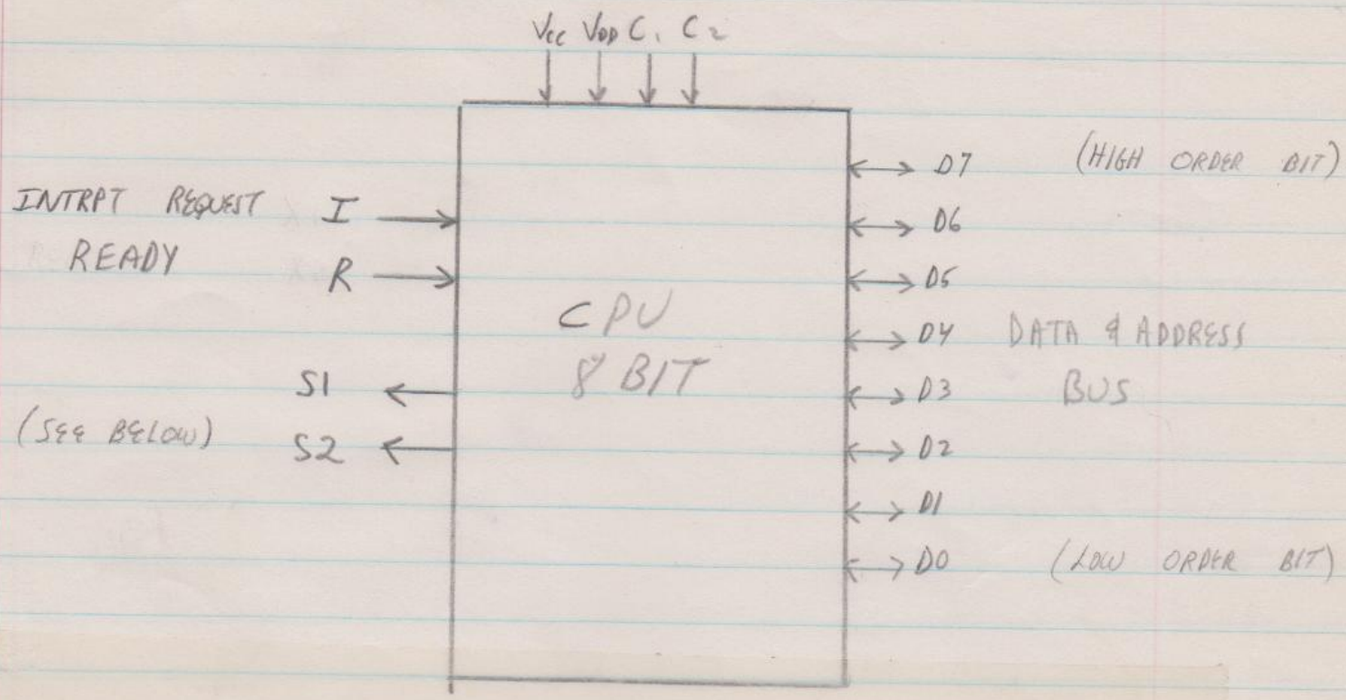
THE PROCESSOR COMMUNICATES OVER AN 8 BIT DATA & ADDRESS BUS AND USES 2 INPUT AND 2 OUTPUT LEADS FOR CONTROL. TIME MULTIPLEXING OF THE DATA BUS ALLOWS CONTROL INFORMATION, 14 BIT ADDRESSES AND DATA TO BE TRANSMITTED BETWEEN THE CPU AND MEMORY.

THE CPU CONTAINS TEN 8-BIT DATA REGISTERS AND A 14-BIT PROGRAM COUNTER. AN 8-BIT PARALLEL BINARY ADDER-SUBTRACTOR IMPLEMENTS ARITHMETIC & LOGICAL OPERATIONS. A MEMORY STACK CONTAINING SEVEN 14-BIT WORDS IS INTERNALLY USED TO STORE PROGRAM SUBROUTINE ADDRESSES.

THE CPU CONTAINS LOGIC TO IMPLEMENT A VARIETY OF REGISTER TRANSFER, ARITHMETIC, CONTROL AND LOGICAL INSTRUCTIONS. SOME INSTRUCTIONS ARE CODED IN ONE BYTE (8 BITS). DATA IMMEDIATE INSTRUCTION USE 2 BYTES; JUMP INSTRUCTIONS UTILIZE 3 BYTES. OPERATING BETWEEN 1 & 2 MICROSECOND CYCLE TIME THE CPU EXECUTES NON MEMORY REFERENCING INSTRUCTIONS IN UNDER 10 MICROSECONDS.

SM
3/4/70

CTC CHIP



S1	S2	STATE	D7	D6	FUNCTION
0	0	WAIT	–	–	–
1	0	OTHER	–	–	–
0	1	SYNCH INTRPT SYNCH	0	0	PCI CYCLE
1	1		1	0	PCR CYCLE
			1	1	PCW CYCLE
			0	1	PCC CYCLE

DURING SYNCH TIME

PCI — INDICATES ADDRESS & DATA CYCLE FOR INSTRUCTION
PCR INDICATES ADDRESS FOR MEMORY READ DATA
PCW INDICATES ADDRESS FOR MEMORY WRITE DATA
PCC INDICATES DATA FOR COMMAND I/O OPERATION

FOR I-O INSTRUCTIONS, D4 AND D5 OF THE INSTRUCTION FIELD ARE 00 FOR READ, 01, 10, OR 11 FOR NON-READ (WRITE OR CONTROL).

INTERRUPT SIGNALS

IF EXTERNAL INPUT SIGNAL "I" IS ENABLED THE CPU RECOGNIZES AN INTERRUPT REQUEST AT SYNCH TIME BY OUTPUTING STATE $S_1 S_2 = 11$ FOR INSTRUCTION FETCH (PCI) CYCLE. ADDRESS1 & ADDRESS2 ARE OUTPUT BUT INTERNALLY THE PROGRAM COUNTER IS NOT ADVANCED. A SUCCESSIVE INSTRUCTION FETCH CYCLE CAN BE USED TO INSERT AN ARBITRARY INSTRUCTION INTO THE INSTRUCTION REGISTER IN THE CPU.

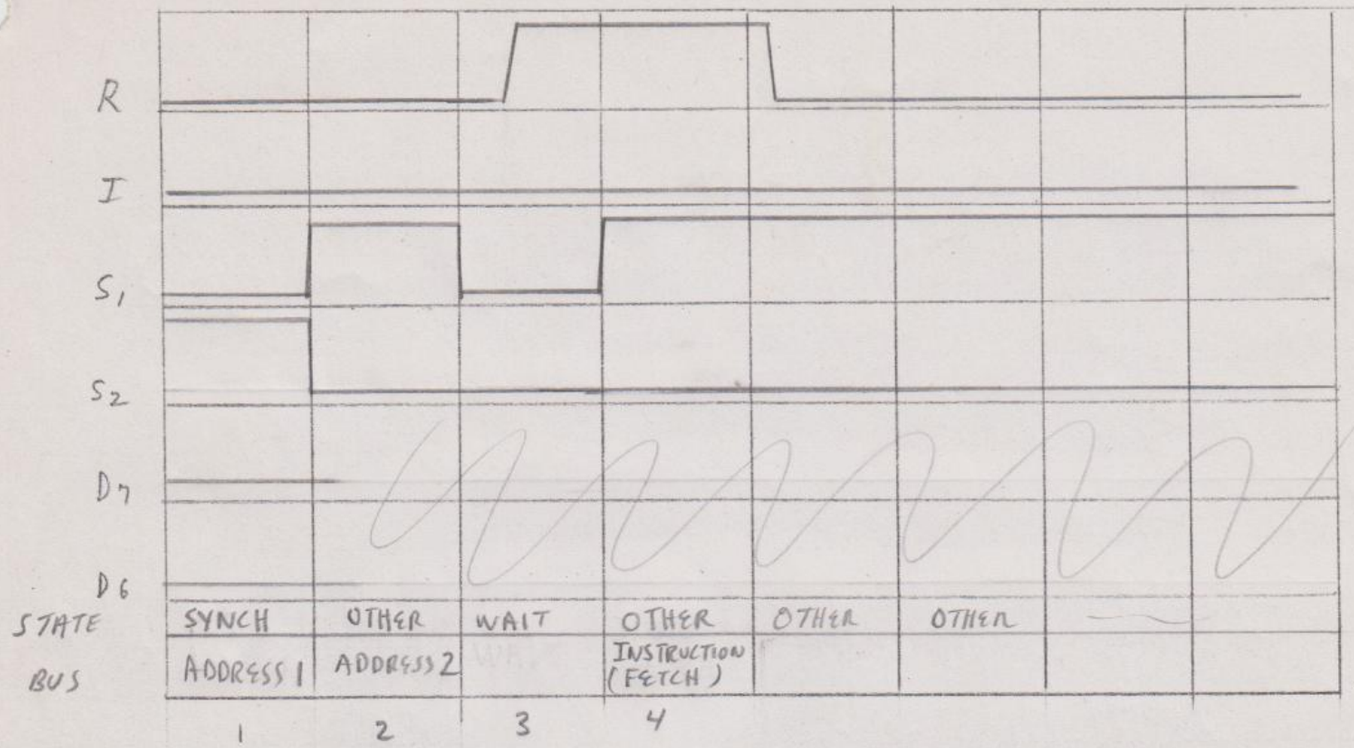
IF A "HALT" IS INSERTED THE CPU ENTERS A STOPPED STATE. IF A "NO-OP" IS INSERTED THE CPU CONTINUES. IF A "JUMP TO 0" IS INSERTED THE PROCESSOR EXECUTES PROGRAM FROM LOCATION 0, ETC.

INTERNAL CPU STATES

THE CPU HAS TWO OPERATING CONDITIONS WHICH ARE DESIGNATED RUNNING AND STOPPED. IN THE RUNNING STATE THE PROGRAM COUNTER SENDS OUT ADDRESSES AND INSTRUCTIONS ARE FETCHED AND EXECUTED. IF A "HALT" COMMAND IS EXECUTED THE CPU ENTERS THE STOPPED STATE. THE CPU REMAINS IN THE STOPPED STATE UNTIL THE INTERRUPT REQUEST SIGNAL (I) IS ENABLED. IN THE STOPPED STATE NO INSTRUCTIONS ARE EXECUTED UNTIL THE INTERRUPT SIGNAL IS ENABLED. WHEN THE INTERRUPT SIGNAL IS ENABLED TO ENTER THE RUNNING STATE, THE CPU STARTS A PCI SEQUENCE BUT DOES NOT INCREMENT THE PROGRAM COUNTER. THIS ALLOWS AN INSTRUCTION TO BE INSERTED INTO THE CPU (SEE INTERRUPTS). THE CPU CAN BE PLACED INTO THE STOPPED STATE BY INTERRUPTING THE CPU AND INSERTING A HALT COMMAND. DURING STOPPED AND WAIT STATES, REGISTERS REALIZED WITH DYNAMIC MEMORY ARE REFRESHED. REFRESH ALSO OCCURS FOR PCI, ER CYCLES.

LOGICAL TIMING DIAGRAM 1

PCI INSTRUCTION FETCH CYCLE (WITH WAIT)

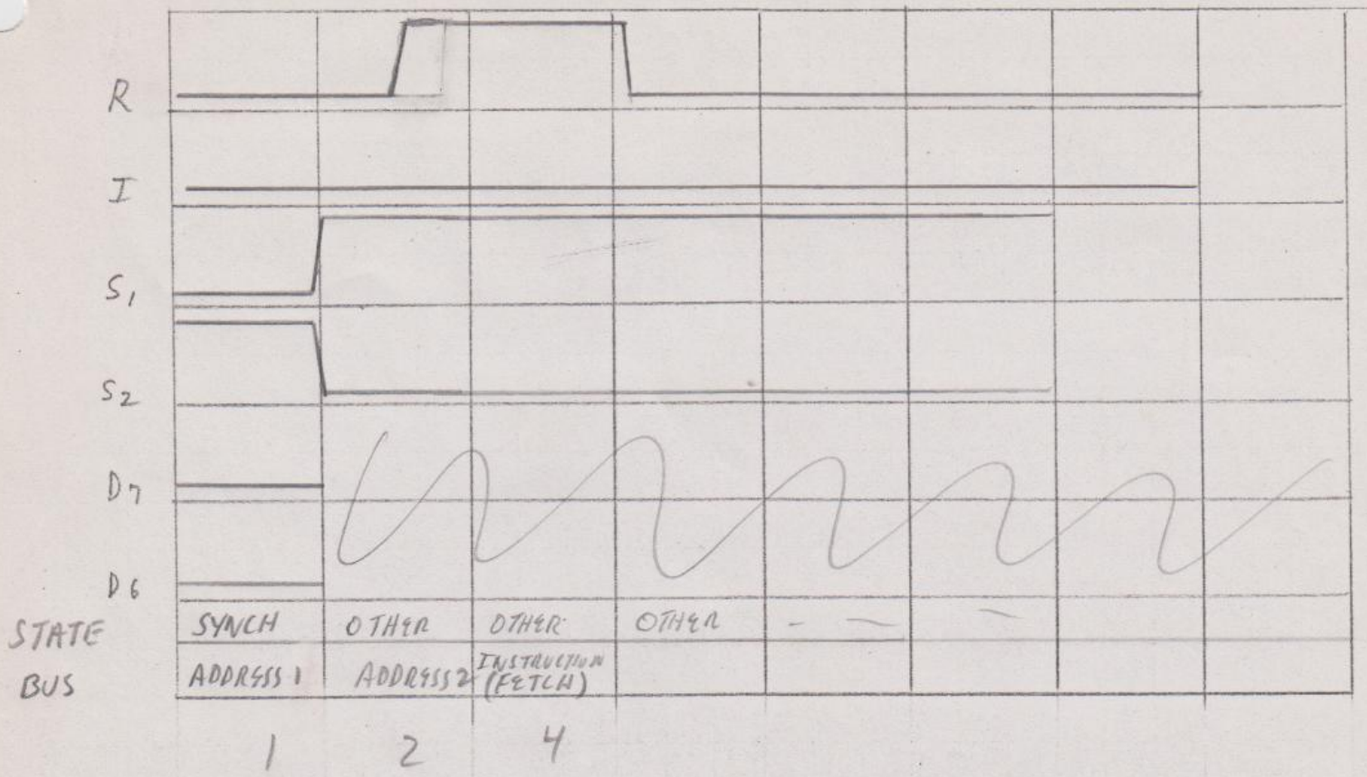


THIS IS STANDARD INSTRUCTION FETCH CYCLE.

1) ADDRESS 1 CONTAINS HIGH ORDER 6 ADDRESS BITS OUTPUT FROM CPU
2) ADDRESS 2 ARE LOW ORDER 8 ADDRESS BITS OUTPUT FROM CPU
3) CPU WAITS FOR MEMORY READY SIGNAL INPUT TO CPU
4) CPU ACCEPTS 8 BIT INSTRUCTION AS INPUT.

LOGICAL TIMING DIAGRAM 2

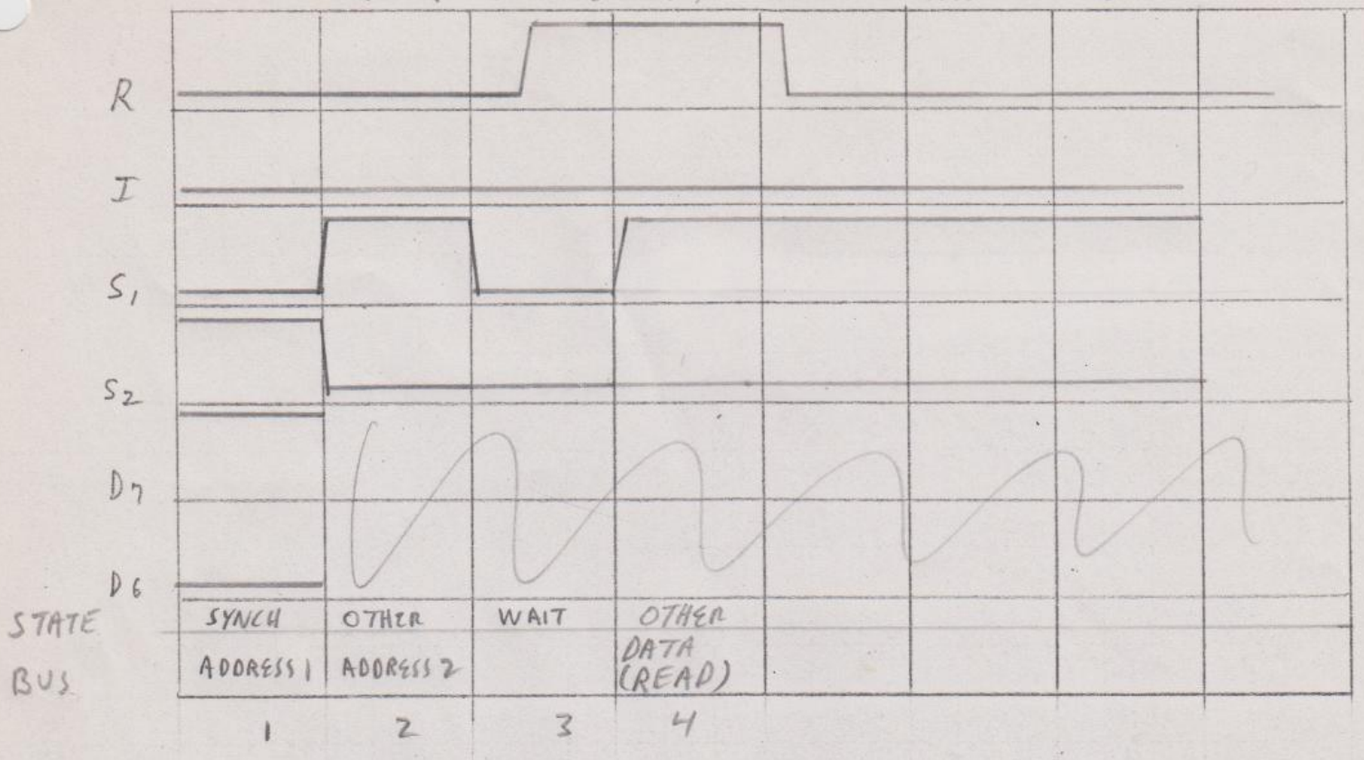
PCI INSTRUCTION FETCH CYCLE (NO WAIT)



SAME AS BEFORE BUT NO WAIT CYCLE

LOGICAL TIMING DIAGRAM 3

PCR MEMORY DATA READ (WITH WAIT)

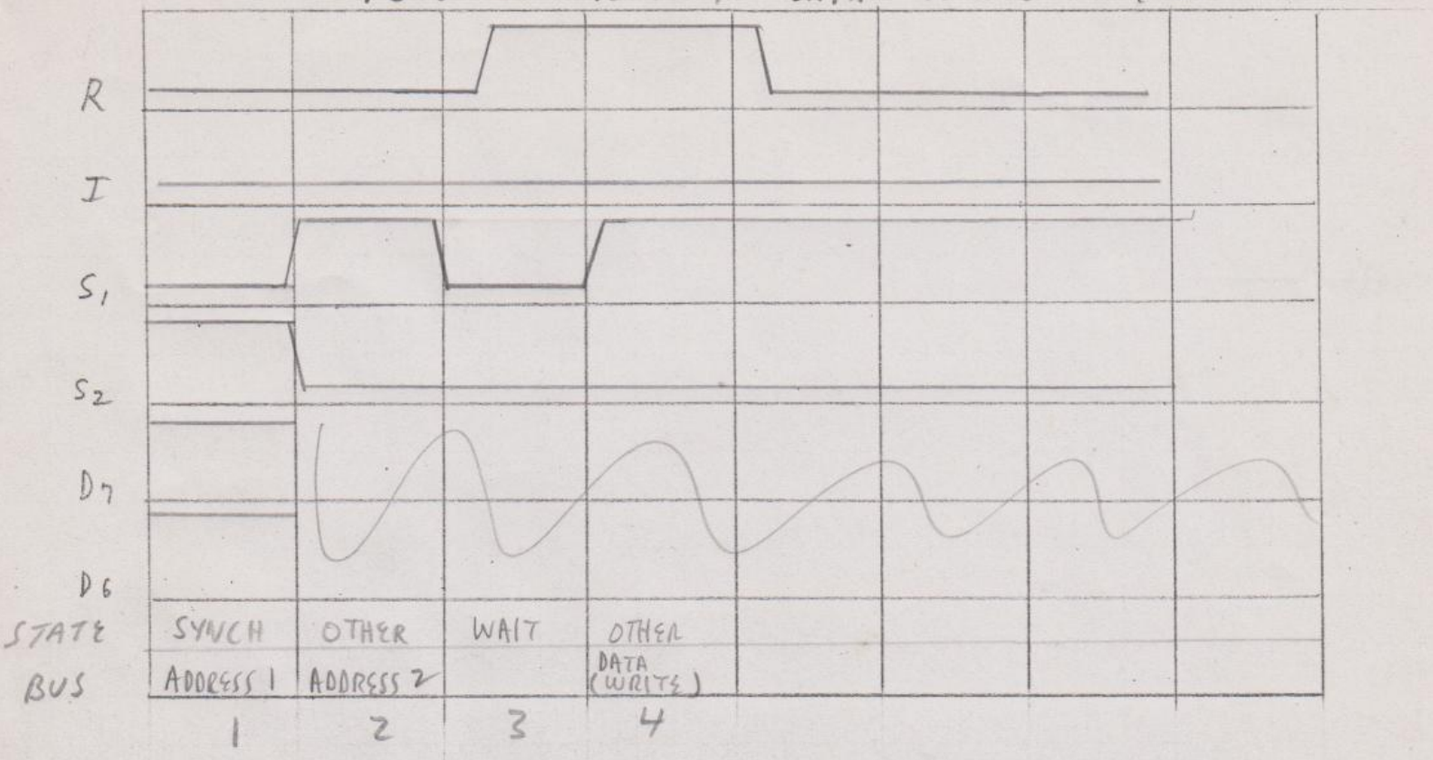


THIS IS STANDARD DATA READ FROM MEMORY (EXECUTION PHASE)

1) ADDRESS1 IS HIGH ORDER 6 ADDRESS BITS OUTPUT
2) ADDRESS2 IS LOW ORDER 8 ADDRESS BITS OUTPUT
3) CPU WAITS FOR MEMORY READY (OPTIONAL)
4) CPU INPUTS 8 DATA BITS INTO CPU

LOGICAL TIMING DIAGRAM 4

PCW MEMORY DATA WRITE (WITH WAIT)

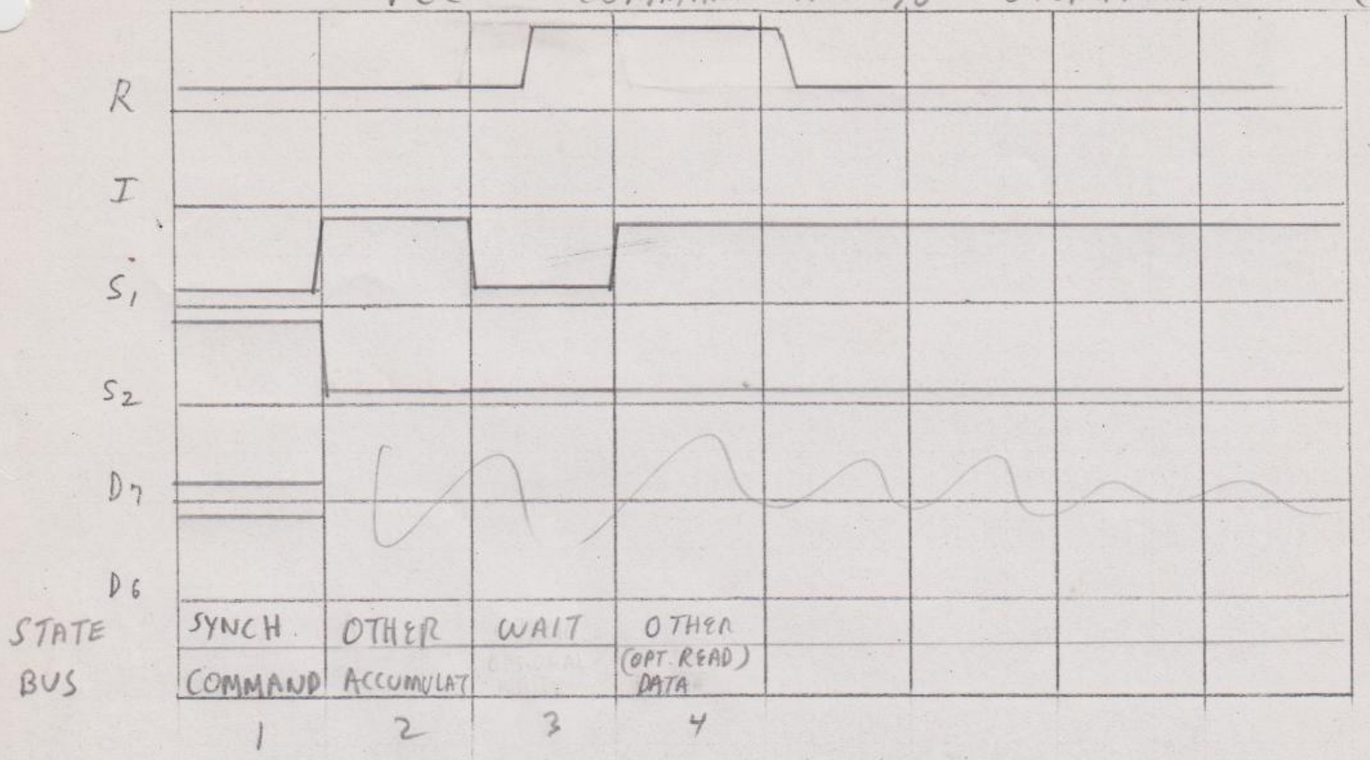


THIS IS STANDARD MEMORY WRITE OPERATION (EXECUTION PHASE)

1) ADDRESS 1 IS HIGH ORDER 6 ADDRESS BITS OUT
2) ADDRESS 2 IS LOW ORDER 8 ADDRESS BITS OUT
3) CPU WAITS FOR MEMORY READY SIGNAL
4) CPU OUTPUTS 8 DATA BITS TO MEMORY

LOGICAL TIMING DIAGRAM 5

PCC COMMAND AND I/O OPERATION (WAIT)



THIS IS COMMAND OPERATION TO I/O UNITS

1) COMMAND OCCURS ON DATA BITS
   D_1 TO D_5

2) CPU OUTPUTS CONTENTS OF ACCUMULATOR

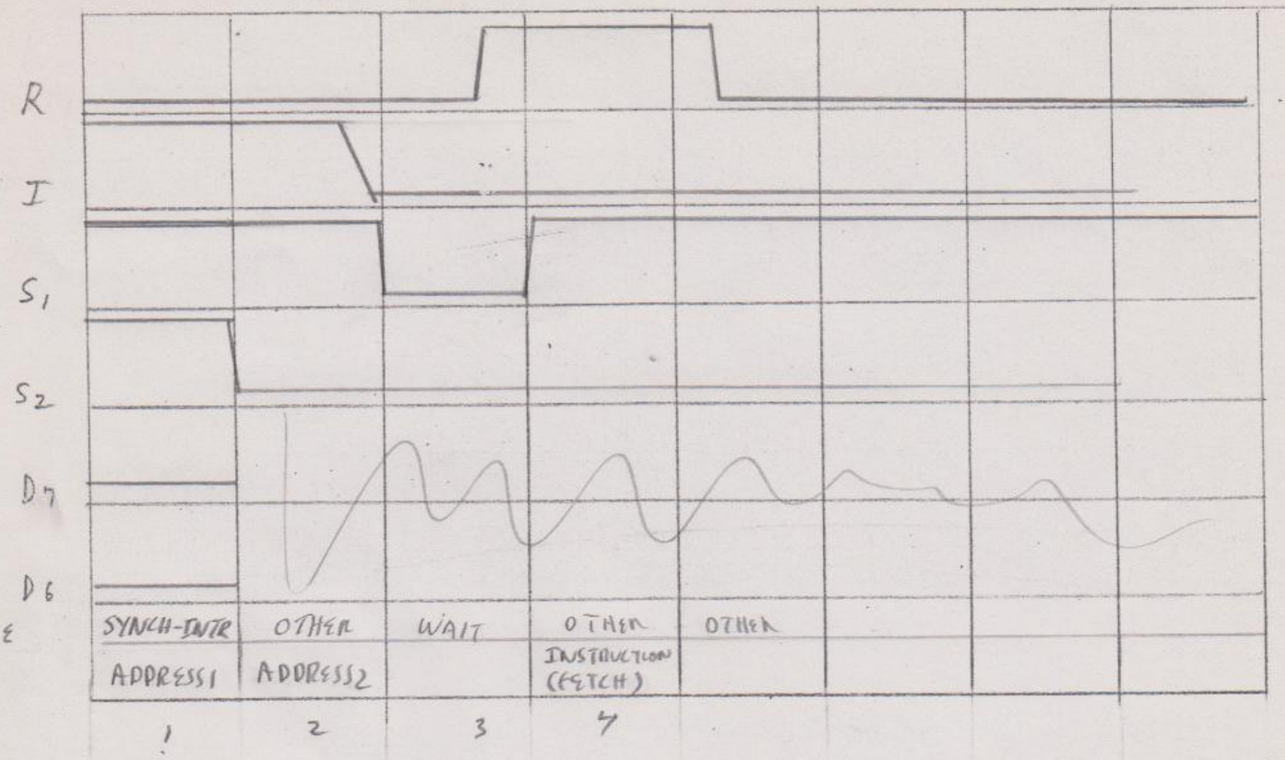
3) CPU WAITS FOR READY SIGNAL (OPTIONAL)

4) CPU WILL INPUT DATA TO ACCUMULATOR
   IF D_4 & D_5 = 00 ON CYCLE 1
   OTHERWISE NO OPERATION PERFORMED ON CYCLE 4

(ABOVE SHOWS EXECUTION PHASE ONLY)

LOGICAL TIMING DIAGRAM 6

PCI INSTRUCTION FETCH INTERRUPT TYPE



SAME AS DIAGRAM 1 BUT INSTRUCTION COUNTER NOT UPDATED

APPENDIX III

INSTRUCTION FORMATS

Source and Destination Codes (s and d): SSS ≠ DDD

0	A	Register	
1	B	Register	
2	C	Register	
3	D	Register	
4	E	Register	
5	H	Register	Memory data
6	L	Register	Address
7	Memory data		USE H&L AS ADDRESS

Operand Codes (p): PPP

0	Add	AD
1	Add with carry	AC
2	Subtract	SU
3	Subtract with carry	SB
4	And	ND
5	Exclusive-or	XR
6	Inclusive-or	OR
7	Compare	CP

FLIP/FLOPS

C_4	C_3			
0	0	0	CARRY = 1	CARRY
0	1	1	ACCUMULATOR IS ZERO	ZERO
1	0	2	ACCUMULATOR IS MINUS	SIGN
1	1	3	ACCUMULATOR PARITY IS ODD	PARITY

W — IF W=0 SHIFT LEFT; W=1 SHIFT RIGHT

I — IF I=1 EXECUTE IF CONDITION TRUE; IF I=0 EXECUTE IF CONDITION FALSE

X — IF X=1 JUMP UNCONDITIONAL; IF X=0 JUMP CONDITIONAL

Y — IF Y=1 STACK ADDRESS; Y=0 DO NOT STACK ADDRESS

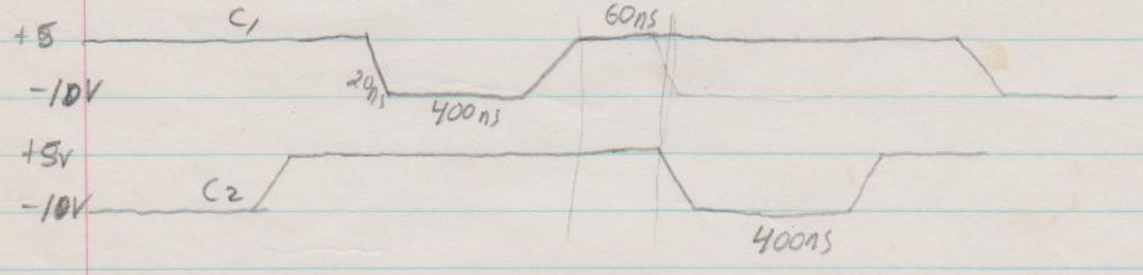
RR MMM IS I/O CONTROL WORD RR=00 MEANS ACC LOAD

INSTRUCTION CODING

	OP	A	B	
1 BYTE	11	DDD	SSS	MOVE SSS TO DDD
"	10	PPP	SSS	ARITHMETIC OPERATION PPP SSS AND ACCUMULATOR
"	00	000	00 -	HALT
	11	111	111	HALT
"	00	I CC	111	RETURN CONDITIONAL
"	00	00 W	010	SHIFT ACCUMULATOR
"	01	RR M	MM I	I/O CONTROL
2 BYTE	00	PPP	100	ARITHMETIC IMMEDIATE
"	00	DDD	110	MOVE IMMEDIATE
3 BYTE	01	I CC	X Y 0	JUMP CONDITIONAL OR UNCONDITIONAL X STACK PUSH OR NOT Y CONDITION CODE CC INVERTED CONDITION I
*OPTIONAL	00	X Y Z	101	RESTART BRANCH TO XYZ 00

CTI CHIP ELECTRICAL SPECIFICATIONS

1. V_{cc} +5
2. V_{DD} -5 to -10
3. SIGNAL LEVELS
   - LOGICAL TRUE (-3V to -5V *
   - LOGICAL FALSE +3.0 to +5V V
   - OUTPUT CURRENT sink 3 ma @ +3.0 VOLT *
     1 ma @ -3.0 VOLT *
4. CLOCKS C_1 & C_2
   +5V $^{+.3}_{-1.0}$ TO -+12 V ± 1V SWING
   RISE & FALL TIMES 20 NS
   60 NS SEPARATION AT +5V
   400 NS DURATION AT -12 V
5. OUTPUTS GENERALLY WILL OCCUR DURING C_1
   TO BE AVAILABLE BY C_2.



6. Bus capacitance should LESS THAN 50 pf

* PRELIMINARY - SUBJECT TO REVISION