COMPUTER TERMINAL CORPORATION

DATAPOINT 2200

REFERENCE MANUAL


Computer Terminal Corporation
DATAPOINT 2200

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PART 1

GENERAL FEATURES

1.1 INTRODUCTION

The Computer Terminal Corporation Datapoint 2200 is an integrated data system consisting of an alphanumeric keyboard for data entry, a cathode ray screen for data display, two digital cassette recorders for bulk data storage, a general purpose digital computer for control, and a communications capability for interface with external devices and communications facilities.

Through programming of the control computer the Datapoint 2200 may be used for an infinite varity of data processing applications.

The achievement of a small computer with integrated keyboard, display, storage and communications at such low cost now makes possible computer sophistication for applications not previously practical - particularly in the computer terminal/data entry/communications area.

This manual describes the specific hardware details of the Datapoint 2200. For information regarding specific applications the Datapoint 2200 Programmers' Guide and specific application manuals should be referred to.

1.2 SYSTEM ELEMENTS

There are four basic system elements in the basic Datapoint 2200 plus the capability of interface to a number of external perpherial devices.

This manual covers the basic elements (c.r.t., keyboard, processor, cassette tape decks) and one external device (communications adaptor).

1.3 CRT DISPLAY

The Datapoint 2200 CRT Display provides the following features:

a. 7" x 2-1/2" viewing area;

b. 960 characters;

c. 80 character by 12 line format;

d. 4/32" x 3/32" character size;

e. Entire 94 character ASCII set;

f. 60 frame per second refresh rate;

g. 5 x 7 matrix character generation;

h. 5 x 7 solid, blinking cursor, alternates with character, nondestructive;

i. P31 green phosphor;

j. Single control line erasure, frame erasure, and page roll-up; and

k. Direct control of all c.r.t. functions by the 2200 processor, providing tab, editing, form control, etc.

1.4 KEYBOARD

The integral keyboard provides a basic 41 key alphanumeric key group, an 11 key numeric group and five system control keys.

The keyboard provides a unique multi-key roll-over characteristic providing maximum ease of typing. Transfer of characters from the keyboard is under control of the 2200 processor. An audible click providing an acoustical feedback to the typist is available under processor control.

A programmable audio "beep" is also provided when it is desired to gain a typist's attention.

1.5 PROCESSOR

The integral processor provides all control functions and includes:

a. 28 different instruction types;

b. 7 addressable registers;

c. 7 deep pushdown stack;

d. 8 bit memory word length;

e. Up to 8192 word memory;

f. Complete parallel I/O system;

g. Automatic power-up restart.

1.6 CASSETTE TAPE DECKS

Two read-write tape decks are provided for program and data storage. The deck accepts Norelco-type cassettes and provides:

a. 47 characters per inch density;

b. Dual-capstan forward-reverse operation;

c. Processor controlled data transfer, direction control, and high-speed rewind.

1.7 COMMUNICATIONS ADAPTOR

The communications adaptor is a unique feature of the Datapoint 2200 system. There are four versions of the adaptor:

a. EIA RS-232 interface for use with external data sets or peripherals;

b. High-level keying interface for connection to telegraph-type communications channels or equipment;

c. 103-type data set interface for direct connection to common carrier lines, and including automatic dialing and answering;

d. 202-type data set interface with 150 bit/sec supervisory channel operation for direct connection to common carrier lines, and including automatic dialing and answering.

The adaptor permits program selection of the desired bit rate, character length, and character set providing the most versatile communications capability yet provided for a remote terminal.

1.8 GENERAL SPECIFICATIONS

The Datapoint 2200 has the following general characteristics:

a. 105-135 v.a.c., 60 cycle, 180 watts, power input;

b. 47 pounds weight;

c. 9-5/8" high, 18-1/2" wide, by 19-5/8" deep outside dimensions;

d. 0° to 50°C (32° to 122°F), 10 to 90 percent relative humidity operation environment.

1.9 OPTIONAL PERIPHERALS

A number of optional peripherals are available (in addition to the communications adaptor) for use with the Datapoint 2200 including a:

a. 132 column, 30 c.p.s. impact page printer; and a

b. IBM compatible magnetic tape deck.

For further information on these devices reference should be made to their respective reference manuals.

PART 2

BASIC PROCESSOR

2.1 PROCESSOR ORGANIZATION

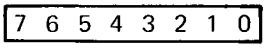
The processor contained in the Datapoint 2200 is comprised of the Arithmetic/Logic Unit, 7 program accessible registers, 2K to 8K words of read/write memory, an instruction decoder and a seven-level hardware pushdown stack used in subroutine type operations.

2.2 ARITHMETIC/LOGIC UNIT

The Arithmetic/Logic Unit is capable of processing both binary integers and logical operands. All arithmetic and logical operations may take place between the A-register and any of the 7 program accessible registers (or between the A-register and memory). The A-register always contains the result of an arithmetic or logic operation, with the other register (or memory cell) begin unaffected. Arithmetic and logic operations affect the Sign, Carry, Zero and Parity Flip-flops.

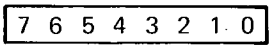
2.3 PROCESSOR REGISTERS

A - The Accumulator register is used to hold the result of all arithmetic and logical instructions. All data transfers into or out of the computer take place through this register.



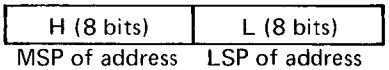
A Register

B, C, D, E - These are general purpose registers which may be used in conjunction with the Accumulator in arithmetic and logical operations. Each register may be loaded from or stored into memory or another register. When used in conjunction with the A and H, L registers, the B, C, D and E registers may function as indexes.



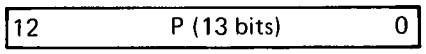
B, C, D, E Registers

H, L - The H and L Registers are utilized to contain respectively the most significant portion (MSP) and least significant portion (LSP) of the address of a memory location being referenced. All memory reference instructions utilize these registers with the exception of CALL and JUMP commands. However, the H and L Registers may be used as general purpose registers when not being used as above.



MSP of address being referenced | LSP of address being referenced

P - The program register or "Location Counter" contains the address of the next instruction to be executed. This register is stored in the pushdown stack upon the execution of a "CALL" instruction and is loaded with the effective address upon execution of a "JUMP", "CALL" or "RETURN" instruction. The P register is 13 bits in length and is capable of addressing up to 8K of memory.



I - The I register is the register which holds the "operation code" of the instruction currently being executed. The contents of I are gated through a decoding network to determine what operation internal or external, is to be performed.

2.4 MEMORY

The basic Datapoint 2200 is supplied with 2048 eight-bit words of memory. Additional modules of 2048 words each may be incorporated with the total memory capacity of the processor being 8192 words. Each 2K memory is made up of 32 individual MOS shift registers with each one having a capacity of 512 bits or 64 eight-bit words. These registers are clocked at a rate of 1.2 MHz. Data is read out in bit serial fashion with one word taking 8 microseconds. During this period of time, two clock pulse times are available for the processor to perform any necessary gating or testing functions.

The Datapoint 2200 memory might be likened to a drum type memory in some respects. It takes approximately 1/2 millisecond for the memory to completely circulate. Thus, if the current instruction referenced a memory location for data access, there would be a 1/2 millisecond delay before that instruction could be completed. However, unlike a drum memory the MOS memory may be stopped during instruction execution so that each succeeding instruction may be read from memory without delay (in 8 usec.).

Physically, instructions require a variable number of cycles for completion. In the first cycle, the instruction is fetched from memory and decoded. If the instruction involves no memory reference, it is then executed within 8 microseconds for a total completion time of 16 microseconds.

"Immediate" type instructions are the same as instructions requiring no memory reference and require a 16 usec. interval for the operand fetch and execute cycle. Jump and Call type instructions require a variable amount of time for execution, depending on the difference between the old and new locations.

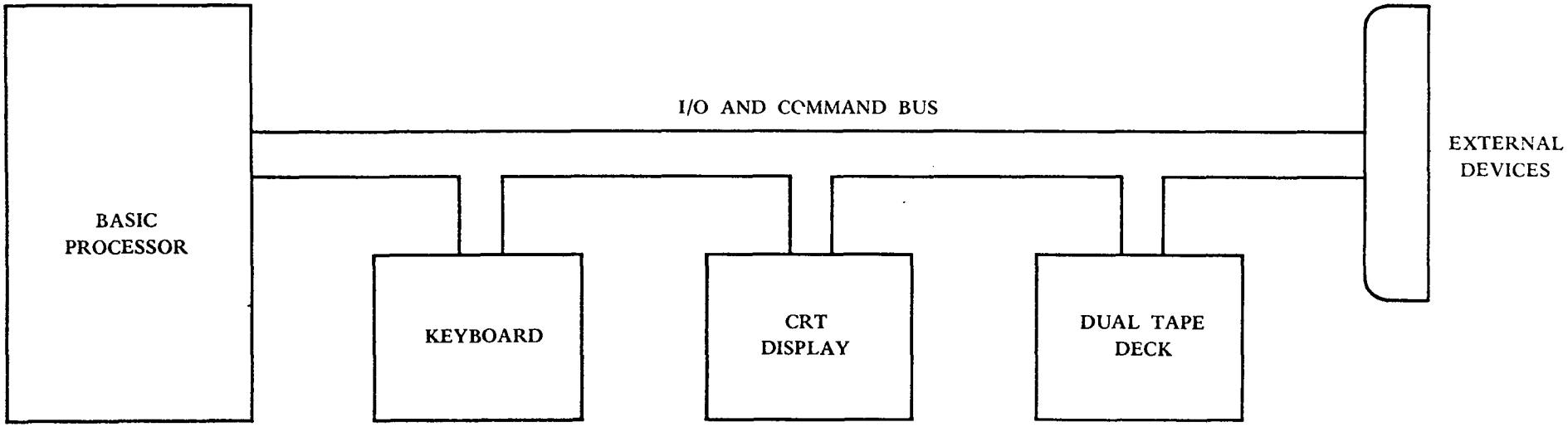


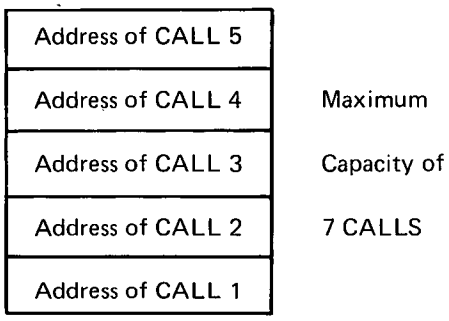
FIGURE 2-1

DATAPOINT 2200
BLOCK DIAGRAM

2.5 PUSHDOWN STACK

A unique feature of a machine this size is the incorporation into the processor's structure of a pushdown stack which is useful in any type of application which requires program subroutines. The stack automatically stores the contents of the P register upon execution of a "CALL" instruction and automatically restores P upon execution of a "RETURN". The stack is a group of "last-in/first-out" registers and has a capacity of 7 CALLS. Note that "CALLS" may be "nested", that is more than one CALL may be made before the execution of a RETURN. The execution of a "RETURN" will cause processor control to be given to the next instruction following the last executed CALL.

Pushdown Stack



2.6 CONTROL FLIP-FLOPS

Also contained in the basic processor are four control flip-flops which reflect the state of the arithmetic logic unit and which may be tested through the execution of a conditional jump, call or return instruction. The flip-flop mnemonics with their associated functions are as follows:

C_f-Carry Flip-flop. Set when an arithmetic operation results in either a carry (add) or borrow (subtract).* The Carry Flip-flop also reflects the state of the most significant bit in the accumulator after completion of a shift right instruction. Likewise, it reflects the state of the accumulator least significant bit after completion of a shift left instruction.

Z_f-Zero Flip-flop. Set when the result of an arithmetic or logical operation is equal to zero.*

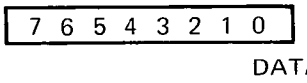
S_f-Sign Flip-flop. This flip-flop reflects the state of bit 7 in the accumulator after an arithmetic type operation.*

P_f-Parity Flip-flop. Indicates the parity or "number of one bits" contained in the accumulator. If this flip-flop is set (true), the A register contains an odd number of one bits; if it is reset (false), the A register contains an even number of one bits.*

*In the event of a compare instruction the contents of the accumulator are not changed; however, the control flip-flops reflect the equivalent of a subtract instruction.

2.7 DATA FORMAT

Data is represented in the Datapoint 2200 in the form of 8-bit binary integers.



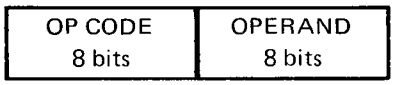
DATA WORD

2.8 INSTRUCTION FORMATS (GENERAL)

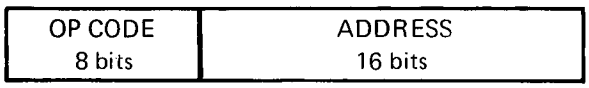
Instruction formats, dependent upon the operation to be performed, may be eight, sixteen or twenty-four bits in length.

Type-1- register to register, memory reference, arithmetic, logical, shift instructions

Type-2- immediate mode instructions



Type-3- JUMP & CALL instructions



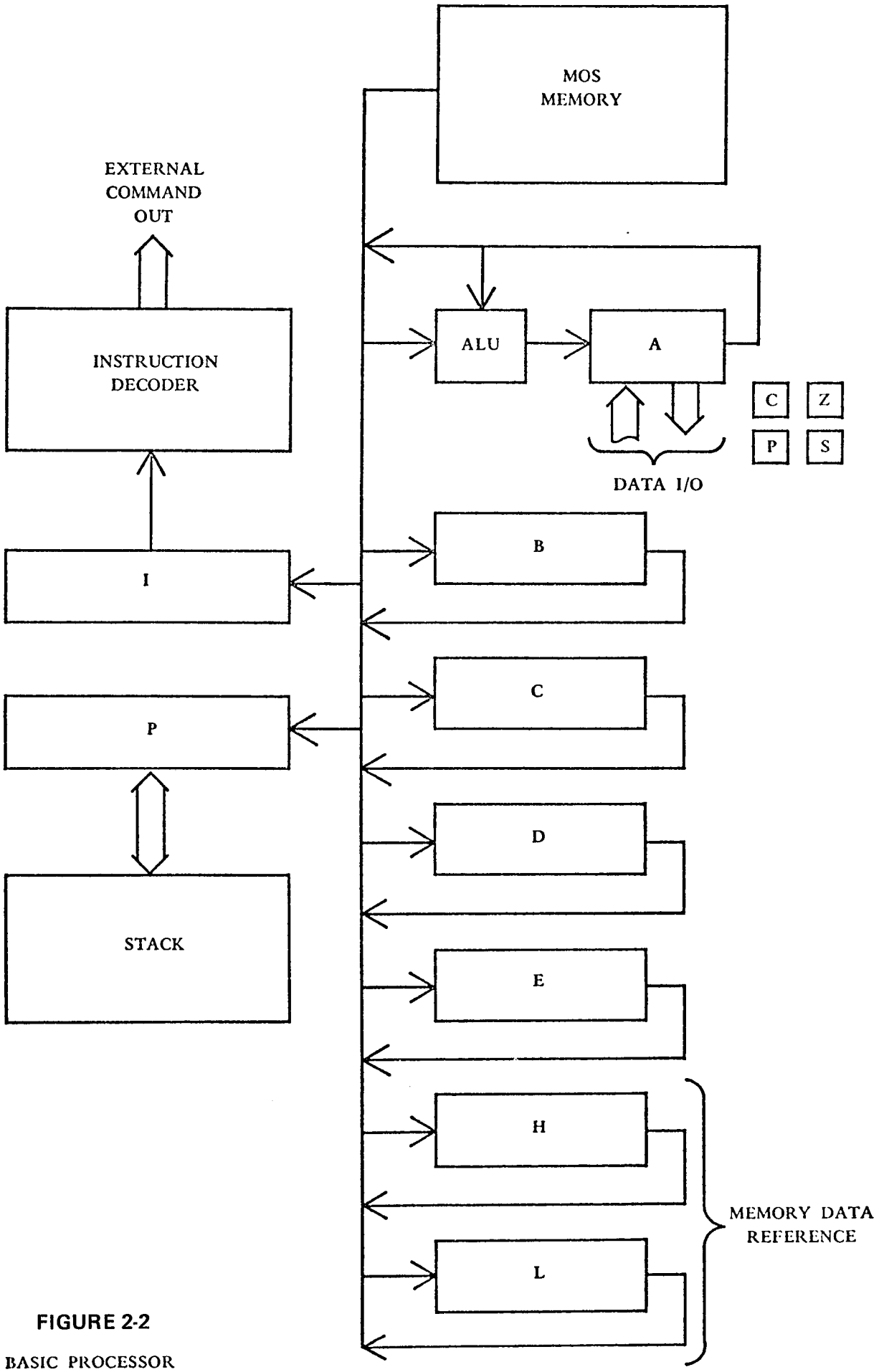


FIGURE 2-2

BASIC PROCESSOR

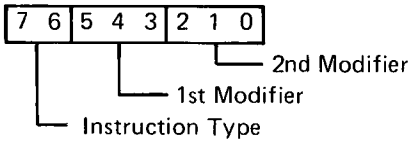
PART 3

INSTRUCTION REPERTOIRE

3.1 PRESENTATION FORMAT

This section gives a detailed description of each of the Datapoint 2200 instructions. The use and operations of each instruction is presented as follows:

FUNCTION:	Mnemonic Code
OPERATION:	Symbolic representation of instruction description.
OP CODE:	Operation Code, expressed in octal.
TIMING:	Execution time. (Times are approximate).
DESCRIPTION:	Definition of function of the instruction.



INSTRUCTION FORMAT: Explanation of the function of each part of the instruction word.

NOTE

Considerations in instruction use and further definition of function.

Symbols and Abbreviations

The following symbols and abbreviations are used in the instruction format:

( )	the contents of
←	is replaced by
→	is transferred to
:	is compared with
A	8 bit arithmetic register (accumulator)
B, C, D, E	8 bit general purpose registers
H	8 bit register used to specify most significant portion of operand address
L	8 bit register used to specify least significant portion of operand address
M	memory location designated by contents of H, L
r	one of the following register designators: A, B, C, D, E, H, L
r_s	designates operand source register (s=0-7)
r_d	designates operand destination register (d=0-7)
V	Logical "OR" operation
⊻	Logical "exclusive-OR" operation
∧	Logical "AND" operation
STACK	Instruction counter (P) pushdown queue
P	Program counter
f_c	Flag flip-flop codes: C_f, Z_f, S_f, P_f
RR	Register to Register
IM	Immediate (from P+1)
MR	Memory Reference (Contents of memory location designated by H, L)
I	Instruction Register

TABLE 3-1

SOURCE AND DESTINATION CODES (s and d)

	s/d	SYMBOLIC CODE	
r_s/r_d	0	A	A Register
	1	B	B Register
	2	C	C Register
	3	D	D Register
	4	E	E Register
	5	H	H Register
	6	L	L Register
M	7	M	Memory location specified by contents of H&L

TABLE 3-2

FLIP-FLOP CODE (f_c)

c	SYMBOLIC CODE	NAME
0	C_f	Carry
1	Z_f	Zero
2	S_f	Sign
3	P_f	Parity

LOAD IMMEDIATE: Lr_d

OP CODE: 0d6 TIMING: 16 usec.

OPERATION: $(P+1) \rightarrow r_d$, $P+2 \rightarrow P$

DESCRIPTION: Transfers the contents of the memory location immediately following the instruction, to the register specified by bits 3-5(d) of the instruction.

INSTRUCTION FORMAT:

P			P+1
7 6	5 4 3	2 1 0	7 0
0	d	6	OPERAND

d: is the destination designator
d=7: is not allowed

NOTE

1. The contents of P+1 are unchanged.
2. None of the Flag Flip-flops are affected.
3. Refer to Table 3-1 for destination codes.

LOAD: Lr_dM, Lr_dr_s, LMr_s

OP CODE: 3ds TIMING: 16 usec. for register to register transfers, 520 usec. for memory reference.

OPERATION: $(M) \rightarrow r_d$ s=7, d≤6 (Lr_dM)
$(r_s) \rightarrow r_d$ s≤6, d≤6 (Lr_dr_s)
$(r_s) \rightarrow M$ s≤6, d=7 (LMr_s)

DESCRIPTION: Transfers the operand from the source specified by bits 0-2 of the instruction word to the destination specified by bits 3-5 of the instruction word.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
3	d	s

d: designates the destination of data.
s: designates the source. If either s or d=7 a memory reference is indicated and the contents of registers H&L specify the address of the memory location.

NOTE

1. The data source is unaffected.
2. s & d both = 7 results in a Halt instruction.
3. None of the Flag Flip-flops are affected by execution of this instruction.
4. s=d results in a NOP, except as stated in Note 2.

ADD IMMEDIATE: AD

OP CODE: 004 TIMING: 16 usec.

OPERATION: (A) + (P+1) → A, P+2 → P

DESCRIPTION: Adds to the contents of the A register the contents of the memory location immediately following the instruction, and retains the sum in the A register. Sets the C_f Flip-flop if ADD overflow occurs, otherwise resets C_f.

INSTRUCTION FORMAT:

P			P+1
7 6	5 4 3	2 1 0	7 0
0	0	4	OPERAND

NOTE

1. The Sign, Zero and Parity Flip-flops will indicate the status of the A register at completion.
2. The contents of P+1 are unchanged.
3. The Carry Flip-flop is cleared at the beginning of this instruction.

ADD WITH CARRY IMMEDIATE: AC

OP CODE: 014 TIMING: 16 usec.

OPERATION: (A) + (P+1) + (C_f) → A, P+2 → P

DESCRIPTION: Adds the C_f bit and the contents of the location immediately following the instruction to the contents of the A register, and retains the sum in the A register. If add overflow occurs, the C_f Flip-flop is set, otherwise C_f is reset.

INSTRUCTION FORMAT:

P			P+1
7 6	5 4 3	2 1 0	7 0
0	1	4	OPERAND

NOTE

1. The Sign, Zero and Parity Flip-flops will indicate the status of the A register at completion.
2. The contents of P+1 remain unchanged.

ADD: ADr_s ADM

OP CODE: 20s TIMING: 16 usec. if RR, 520 usec. if MR

OPERATION: (A) + (r_s) → A or (A) + (M) → A

DESCRIPTION: This instruction is identical to ADD IMMEDIATE with the exception of operand source.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
2	0	s

s: specifies the operand source. Refer to Table 3-1 for source codes.

ADD WITH CARRY: ACr_s ACM

OP CODE: 21s TIMING: 16 usec. if RR, 520 usec. if MR

OPERATION: (A) + (C_f) + (r_s) → A or (A) + (C_f) + (M) → A

DESCRIPTION: This instruction is identical to ADD WITH CARRY IMMEDIATE with the exception of operand souce.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
2	1	s

s: specifies the operand source. Refer to Table 3-1 for source codes.

SUBTRACT IMMEDIATE: SU

OP CODE: 024 TIMING: 16 usec.

OPERATION: (A) - (P+1) → A, P+2 → P

DESCRIPTION: Subtracts the contents of the memory location immediately following the instruction from the contents of the A register, and retains the difference in the A register. The C_f Flip-flop is set if underflow occurs.

INSTRUCTION FORMAT:

P			P+1
7 6	5 4 3	2 1 0	7 0
0	2	4	OPERAND

NOTE

1. The contents of P+1 is unchanged.
2. The Zero, Sign, and Parity Flip-flops represent the status of the A register at the completion of this instruction.

SUBTRACT WITH BORROW IMMEDIATE: SB

OP CODE: 034 TIMING: 16 usec.

OPERATION: (A) - (P+1) - (C_f) → A, P+2 → P

DESCRIPTION: Subtracts the contents of the memory location immediately following the instruction and the C_f bit, from the contents of the A register. Sets the C_f bit if underflow occurs, otherwise resets C_f.

INSTRUCTION FORMAT:

P			P+1
7 6	5 4 3	2 1 0	7 0
0	3	4	OPERAND

NOTE

1. The contents of P+1 are unchanged.
2. The Zero, Sign, and Parity Flip-flops represent the status of the A register at the completion of this instruction.

SUBTRACT: SUr_s SUM

OP CODE: 22s TIMING: 16 usec. if RR, 520 usec. if MR

OPERATION: (A) - (r_s) → A or (A) - (M) → A

DESCRIPTION: This instruction is identical to SUBTRACT IMMEDIATE with the exception of operand source.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
2	2	s

s: specifies the operand source. Refer to Table 3-1 for source codes.

SUBTRACT WITH BORROW: SBr_s SBM

OP CODE: 23s TIMING: 16 usec. if RR, 520 usec. if MR

OPERATION: (A) - (r_s) - (C_f) → A or (A) - (M) - (C_f) → A

DESCRIPTION: This instruction is identical to SUBTRACT WITH BORROW IMMEDIATE with the exception of operand source.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
2	3	s

s: specifies the operand source. Refer to Table 3-1 for source codes.

AND IMMEDIATE: ND

OP CODE: 044 TIMING: 16 usec.

OPERATION: (P+1) $\wedge$ (A) → A, P+2 → P

DESCRIPTION: Forms the logical product of the contents of the A register with the contents of the memory location immediately following the instruction, and places the results in the A register.

INSTRUCTION FORMAT:

P			P+1
7 6	5 4 3	2 1 0	7 0
0	4	4	OPERAND

NOTE

1. The Carry Flip-flop will be reset upon completion of the operation.
2. The Zero, Sign, and Parity Flip-flops will represent the status of the A register upon completion of the operation.

SAMPLE OPERATION:

(A Reg)	0	0	1	1
(P+1)	0	1	0	1
(A Reg)	0	0	0	1

OR IMMEDIATE: OR

OP CODE: 064 TIMING: 16 usec.

OPERATION: (A) V (P+1) → A, P+2 → P

DESCRIPTION: Forms the logical sum of the contents of the A register and the contents of the memory location immediately following the instruction, and places the result in the A register.

INSTRUCTION FORMAT:

P			P+1
7 6	5 4 3	2 1 0	7 0
0	6	4	OPERAND

NOTE

1. The Carry Flip-flop will be reset at conclusion.
2. The Zero, Sign, and Parity Flip flops will represent the status of the A register at completion of the operation.

SAMPLE OPERATION:

(A Reg)	0	0	1	1
(P+1)	0	1	0	1
(A Reg)	0	1	1	1

AND: NDr$_s$, NDM

OP CODE: 24s TIMING: 16 usec. if RR, 520 usec. if MR

OPERATION: (A) $\wedge$ (r_s) → A, or (A) $\wedge$ (M) → A

DESCRIPTION: This instruction is identical to AND IMMEDIATE with the exception of operand source.

INSTRUCTION FORMAT:

7 6	5 4 3	2 1 0
2	4	s

s: specifies the operand source. Refer to Table 3-1 for source codes.

OR: ORr$_s$ ORM

OP CODE: 26s TIMING: 16 usec. if RR, 520 usec. if MR

OPERATION: (A) V (r_s) → A, or (A) V (M) → A

DESCRIPTION: This instruction is identical to OR IMMEDIATE with the exception of operand source.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
2	6	s

s: specifies the operand source. Refer to Table 3-1 for source codes.

EXCLUSIVE OR IMMEDIATE: XR

OP CODE: 054 TIMING: 16 usec.

OPERATION: (A) $\forall$ (P+1) → A, P+2 → P

DESCRIPTION: The logical difference of the contents of the A register and the contents of the memory location immediately following the instruction is formed, and the result replaces the contents of the A register.

INSTRUCTION FORMAT:

P			P+1
7 6	5 4 3	2 1 0	7 0
0	5	4	OPERAND

NOTE

1. The Carry Flip-flop will be reset at conclusion.
2. The Zero, Sign and Parity Flip-flops will represent the status of the A register upon completion of the operation.

SAMPLE OPERATION:

(A Reg)	0	0	1	1
(P+1)	0	1	0	1
(A Reg)	0	1	1	0

COMPARE IMMEDIATE: CP

OP CODE: 074 TIMING: 16 usec.

OPERATION: (A) : (P+1), P+2 → P

DESCRIPTION: Compares the contents of the A register with the contents of the memory location immediately following the instruction. The flag flip-flops assume the same state as they would for a Subtract instruction.

INSTRUCTION FORMAT:

P			P+1
7 6	5 4 3	2 1 0	7 0
0	7	4	OPERAND

NOTE

1. The contents of the A register are unaffected.

EXCLUSIVE OR: XRr_s XRM

OP CODE: 25s TIMING: 16 usec. if RR, 520 usec. if MR

OPERATION: (A) V (r_s) → A, (A) V (M) → A

DESCRIPTION: This instruction is identical to EXCLUSIVE OR IMMEDIATE with the exception of operand source.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
2	5	s

s: specifies the operand source. Refer to Table 3-1 for source codes.

COMPARE: CPr_s CPM

OP CODE: 27s TIMING: 16 usec. if RR, 520 usec. if MR

OPERATION: (A) : (r_s) or (A) : (M)

DESCRIPTION: This instruction is identical to COMPARE IMMEDIATE with the exception of operand source.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
2	7	s

s: specifies the operand source. Refer to Table 3-1 for source codes.

UNCONDITIONAL JUMP: JMP

OP CODE: 104
TIMING: Variable*
OPERATION: (P+1, P+2) → P
DESCRIPTION: An unconditional transfer of control. The contents of P+1 represent the least significant portion of the address, while the contents of P+2 represent the most significant portion.

INSTRUCTION FORMAT:

P			P+1	P+2
7 6	5 4 3	2 1 0	7 0	7 0
1	0	4	LSP	MSP
	OP CODE		ADDRESS	

The three high order bits in the address are ignored, the remaining 13 bits specify the address to which control is to be transferred.

NOTE

*Timing is variable dependent upon cyclic difference between instruction and effective address locations.

JUMP IF CONDITION TRUE: JTf_c

OP CODE: 1(c+4)0
TIMING: Variable if condition true, 24 usec. if condition false.
OPERATION: If (f_c=TRUE), (P+1 , P+2) → P. Otherwise, P+3 → P.
DESCRIPTION: Examines the designated flip-flop. If set, transfers control to the address designated by the contents of the two memory locations immediately following the instruction. If the selected flip-flop is reset, executes the next sequentially available instruction.

INSTRUCTION FORMAT:

P			P+1	P+2
7 6	5 4 3	2 1 0	7 0	7 0
1	c+4	0	LSP	MSP
	OP CODE		ADDRESS	

c: designates which flip-flop condition is to be tested. Refer to Table 3-2 for list of Flip-flop codes.

NOTE

1. The condition of the selected Flip-flop is unchanged by this instruction.

JUMP IF CONDITION FALSE: JFf_c

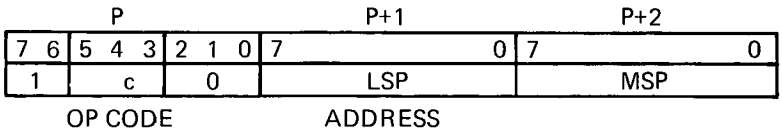
OP CODE: 1c0

TIMING: Variable if condition false, 24 usec. if condition true.

OPERATION: If (f_c=FALSE), (P+1, P+2) → P. Otherwise P+3 → P.

DESCRIPTION: Examines the designated flip-flop. If reset, transfers control to the address designated by the contents of the two memory locations immediately following the instruction. If the selected flip-flop is set, executes the next sequentially available instruction.

INSTRUCTION FORMAT:



c: designates which flip-flop (condition) is to be tested. Refer to Table 3-2 for list of flip-flop codes.

NOTE

1. The condition of the selected flip-flop is unchanged by this instruction.

SUBROUTINE CALL: CALL

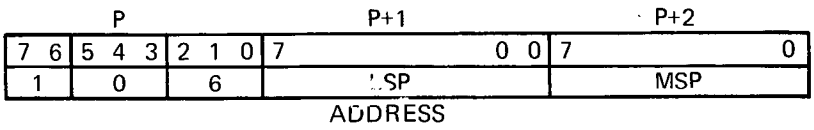
OP CODE: 106

TIMING: Variable

OPERATION: P+3 → STACK, (P+1, P+2) → P

DESCRIPTION: Transfers the address of the next sequentially available instruction to the Pushdown Stack, and transfer control to the address specified by the contents of the two memory locations immediately following the Op Code.

INSTRUCTION FORMAT:



NOTE

1. The Stack is open-ended in operation. If it is overfilled, the deepest address will be lost.

CONDITIONAL SUBROUTINE CALL

IF CONDITION TRUE: CTf_c

OP CODE: 1(c+4)2

TIMING: Variable if condition true, 24 usec. if condition false.

OPERATION: If (f_c=TRUE), P+3 → STACK, (P+1, P+2) → P. Otherwise, P+3 → P.

DESCRIPTION: Examines the designated flip-flop. If set, transfers the address of the next sequentially available instruction to the pushdown stack, and transfers control to the address of the two memory locations immediately following the Op Code. If the selected flip-flop is reset, executes the next sequentially available instruction.

INSTRUCTION FORMAT:

			P+1	P+2
7 6	5 4 3	2 1 0	7 0	7 0
1	c+4	2	LSP	MSP
			ADDRESS	

c: designates which flip-flop (condition) is to be tested.

NOTE

1. The condition of the selected flip-flop is unchanged by this instruction.
2. The stack is open-ended in operation. If it is overfilled, the deepest address will be lost.
3. Refer to Table 3-2 for list of flip-flop codes.

CONDITIONAL SUBROUTINE CALL

IF CONDITION FALSE: CFf_c

OP CODE: 1c2

TIMING: Variable if condition false, 24 usec. if condition true.

OPERATION: If (f_c=FALSE), P+3 → STACK, (P+1, P+2) → P.

DESCRIPTION: Examines the designated flip-flop. If reset, transfers the address of the next sequentially available instruction to the pushdown stack, and transfers control to the address of the two memory locations immediately following the Op Code. If the selected flip-flop is set, executes the next sequentially available instruction.

INSTRUCTION FORMAT:

			P+1	P+2
7 6	5 4 3	2 1 0	7 0	7 0
1	c	2	LSP	MSP
			ADDRESS	

c: designates which flip-flop (condition) is to be tested.

NOTE

1. The condition of the selected flip-flop is unchanged by this instruction.
2. The stack is open-ended in operation. If it is overfilled, the deepest address will be lost.
3. Refer to Table 3-2 for list of flip-flop codes.

SUBROUTINE RETURN: RETURN

OP CODE: 007
TIMING: Variable
OPERATION: (STACK) → P
DESCRIPTION: Transfer control to the address specified by the most recent entry in the Pushdown Stack. Deletes the most recent entry from the Stack.

INSTRUCTION FORMAT:

P

7 6	5 4 3	2 1 0
0	0	7

NOTE

1. The effect of attempting more "RETURN" than the Stack is capable of handling is undefined.

CONDITIONAL SUBROUTINE RETURN

IF CONDITION TRUE: RTf_c

OP CODE: 0(c+4)3
TIMING: Variable if condition true, 16 usec. if condition false.
OPERATION: If (f_c=TRUE), Stack → P. Otherwise P+3 → P
DESCRIPTION: Examines the designated flip-flop. If set, transfers control to the address specified by the most recent entry in the pushdown stack. Deletes the most recent entry in the stack. If the selected flip-flop is reset, executes the next sequentially available instruction.

INSTRUCTION FORMAT:

7 6	5 4 3	2 1 0
1	c+4	3

c: designates which flip-flop (condition) is to be tested.

NOTE

1. The condition of the selected flip-flop is unchanged by this instruction.
2. The effect of attempting more "RETURN" than the stack is capable of handling is undefined.
3. Refer to Table 3-2 for list of flip-flop codes.

CONDITIONAL SUBROUTINE RETURN

IF CONDITION FALSE: RFf_c

OP CODE: 0c3
TIMING: Variable if condition false, 16 usec. if condition true.
OPERATION: If (f_c= FALSE), Stack → P. Otherwise, P+3 → P
DESCRIPTION: Examines the designated flip-flop. If reset, transfers control to the address specified by the most recent entry in the stack. If the selected flip-flop is set, executes the next sequentially available instruction.

INSTRUCTION FORMAT:

7 6	5 4 3	2 1 0
1	c	3

c: designates which flip-flop (condition) is to be tested.

NOTE

1. The condition of the selected flip-flop is unchanged by this instruction.
2. The effect of attempting more "RETURN" than the stack is capable of handling is undefined.
3. Refer to Table 3-2 for list of flip-flop codes.

SHIFT RIGHT CIRCULAR: SRC

OP CODE: 012 TIMING: 16 usec.

OPERATION: $A_m \rightarrow A_{m-1}$, $A_0 \rightarrow A_7$, $A_0 \rightarrow C_f$

DESCRIPTION: Shifts the contents of the A register right in a circular fashion. Shifts the least significant bit into the most significant bit position. Upon completion of the operation, the Carry Flip-flop is equal to the most significant bit.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
0	1	2

NOTE

None of the flag flip-flops other than C_f is affected by this instruction.

SHIFT LEFT CIRCULAR: SLC

OP CODE: 002 TIMING: 16 usec.

OPERATION: $A_m \rightarrow A_{m+1}$, $A_7 \rightarrow A_0$, $A_7 \rightarrow C_f$

DESCRIPTION: Shifts the contents of the A register left in a circular fashion. Shifts the most significant bit into the least significant bit position. Upon completion of the operation, the Carry Flip-flop is equal to the least significant bit.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
0	0	2

NOTE

None of the flag flip-flops other than C_f is affected by this instruction.

NO OPERATION: NOP

OP CODE: 300 TIMING: 16 usec.

OPERATION: P+1 → P

DESCRIPTION: No instruction is executed.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
3	0	0

HALT: HALT

OP CODE: 000,001,377 TIMING: Execution Stops

OPERATION:

DESCRIPTION: The computer halts. When the START buttom on the console is depressed, operation resumes at P+1.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
0	0	0
0	0	1
3	3	7

INPUT: INPUT

OP CODE: 101 TIMING: 16 usec.

OPERATION: (I/O Bus) → A

DESCRIPTION: Transfers the contents of the I/O Bus to the A register.

INSTRUCTION FORMAT:

P		
7 6	5 4 3	2 1 0
1	0	1

EXTERNAL COMMAND: **EX (exp)**

OP CODE: 121-177 depending on the specific command being executed.

TIMING: 16 usec.

OPERATION: Performs I/O control functions according to (exp)

DESCRIPTION: These instructions perform the functions necessary for control of the I/O system and external devices. Many of these functions are specifically related to operation of particular devices. The device oriented commands for the Keyboard, CRT Display, Cassette Tapes, and Communications Interface are explained in the sections covering these devices.

INSTRUCTION FORMAT:

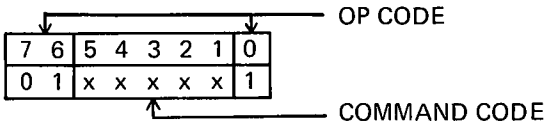


Table 3-3 is a list of External Commands used. For a detailed discussion of their use, reference should be made to Part 4 (Input/Output Operations) and to descriptions of the separate external devices.

TABLE 3-3

EXTERNAL COMMANDS

EX (exp)

COMMAND NUMBER	(exp)	OCTAL CODE	COMMAND	DESCRIPTION	DEVICE ADDRESS
1	ADR	121	Address	Selects device specified by A-register	ALL
2	STATUS	123	Sense Status	Connects selected device status to input lines	
3	DATA	125	Sense Data	Connects selected device data to input lines	
4	WRITE	127	Write Strobe	Signals selected device that output data word is on output lines	
5	COM1	131	Command 1	Outputs a control function to selected device	
6	COM2	133	Command 2	Outputs a control function to selected device	
7	COM3	135	Command 3	Outputs a control function to selected device	
8	COM4	137	Command 4	Outputs a control function to selected device	ALL
9	--	141	(Unassigned)	--	--
10	--	143	(Unassigned)	--	--
11	--	145	(Unassigned)	--	--
12	--	147	(Unassigned)	--	--

TABLE 3-3

EXTERNAL COMMANDS

EX (exp)

(Continued)

COMMAND NUMBER	(exp)	OCTAL CODE	COMMAND	DESCRIPTION	DEVICE ADDRESS
13	BEEP	151	Beep	Activates tone producing mechanism	341
14	CLICK	153	Click	Activates audible click producing mechanism	341
15	DECK1	155	Select Deck 1	Connects deck 1 to I/O bus	360
16	DECK2	157	Select Deck 2	Connects deck 2 to I/O bus	|
17	RBK	161	Read Block	Enables read circuitry and sets tape in forward motion	|
18	WBK	163	Write Block	Enables write circuitry and sets tape in forward motion	360
19	--	165	(Unassigned)	--	--
20	BSP	167	Backspace One Block	Backs up the selected tape one record	360
21	SF	171	Slew Forward	Sets selected tape deck in forward motion	|
22	SB	173	Slew Backward	Sets selected tape deck in backward motion	|
23	REWIND	175	Rewind	Rewinds the selected deck to beginning of tape	|
24	TSTOP	177	Stop Tape	Halts motion of the selected tape deck	360

TABLE 3-4

INSTRUCTION REPERTOIRE

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
000	HALT	050		120	JFS
001	HALT	051		121	EX ADR
002	SLC	052		122	CFS
003	RFC	053	RTZ	123	EX STATUS
004	AD	054	XR	124	
005		055		125	EX DATA
006	LA	056	LH	126	
007	RETURN	057		127	EX WRITE
010		060		130	JFP
011		061		131	EX COM1
012	SRC	062		132	CFP
013	RFZ	063	RTS	133	EX COM2
014	AC	064	OR	134	
015		065		135	EX COM3
016	LB	066	LL	136	
017		067		137	EX COM4
020		070		140	JTC
021		071		141	
022		072		142	CTC
023	RFS	073	RTP	143	
024	SU	074	CP	144	
025		075		145	
026	LC	076		146	
027		077		147	
030		100	JFC	150	JTZ
031		101	INPUT	151	EX BEEP
032		102	CFC	152	CTZ
033	RFP	103		153	EX CLICK
034	SB	104	JMP	154	
035		105		155	EX DECK1
036	LD	106	CALL	156	
037		107		157	EX DECK2
040		110	JFZ	160	JTS
041		111		161	EX RBK
042		112	CFZ	162	CTS
043	RTC	113		163	EX WBK
044	ND	114		164	
045		115		165	
046	LE	116		166	
047		117		167	EX BSP

TABLE 3-4

INSTRUCTION REPERTOIRE

(Continued)

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
170	JTP	240	NDA	310	LBA
171	EX SF	241	NDB	311	
172	CTP	242	NDC	312	LBC
173	EX SB	243	NDD	313	LBD
174		244	NDE	314	LBE
175	EX REWND	245	NDH	315	LBH
176		246	NDL	316	LBL
177	EX TSTOP	247	NDM	317	LBM
200	ADA	250	XRA	320	LCA
201	ADB	251	XRB	321	LCB
202	ADC	252	XRC	322	
203	ADD	253	XRD	323	LCD
204	ADE	254	XRE	324	LCE
205	ADH	255	XRH	325	LCH
206	ADL	256	XRL	326	LCL
207	ADM	257	XRM	327	LCM
210	ACA	260	ORA	330	LDA
211	ACB	261	ORB	331	LDB
212	ACC	262	ORC	332	LDC
213	ACD	263	ORD	333	
214	ACE	264	ORE	334	LDE
215	ACH	265	ORH	335	LDH
216	ACL	266	ORL	336	LDL
217	ACM	267	ORM	337	LDM
220	SUA	270	CPA	340	LEA
221	SUB	271	CPB	341	LEB
222	SUC	272	CPC	342	LEC
223	SUD	273	CPD	343	LED
224	SUE	274	CPE	344	
225	SUH	275	CPH	345	LEH
226	SUL	276	CPL	346	LEL
227	SUM	277	CPM	347	LEM
230	SBA	300	NOP	350	LHA
231	SBB	301	LAB	351	LHB
232	SBC	302	LAC	352	LHC
233	SBD	303	LAD	353	LHD
234	SBE	304	LAE	354	LHE
235	SBH	305	LAH	355	
236	SBL	306	LAL	356	LHL
237	SBM	307	LAM	357	LHM

TABLE 3-4

INSTRUCTION REPERTOIRE

(Continued)

OP CODE	MNEMONIC	OP CODE	MNEMONIC	OP CODE	MNEMONIC
360	LLA	370	LMA		
361	LLB	371	LMB		
362	LLC	372	LMC		
363	LLD	373	LMD		
364	LLE	374	LME		
365	LLH	375	LMH		
366		376	LML		
367	LLM	377	HALT		

NOTE

OP Codes shown without Mnemonics are undefined.

PART 4

INPUT/OUTPUT OPERATIONS

4.1 GENERAL

The versatile input/output capability of the Datapoint 2200 permits it to communicate with external devices (such as the 2200 communications adaptor) through a parallel I/O system. The keyboard, c.r.t. and tape decks that are an integral part of the Model 2200 perform all operations over the same I/O system as external devices.

4.2 INPUT/OUTPUT INSTRUCTIONS

Two types of instructions provide for I/O operations. One is the INPUT command (see section 3) which, upon execution, transfers whatever is on the input bus to the A-register. The second is the EXTERNAL command which is sub-divided into 24 separate command operations (8 of which are available to devices physically external to the Model 2200). Each EXTERNAL command produces a strobe pulse which may be used for control external to the processor. The actual control functions assigned to each external command are listed in Table 3-3.

4.3 INPUT/OUTPUT CABLE

The parallel I/O cable carries data, input strobe, external commands, and power between the 2200 processor and external devices connected to it. A complete I/O system is structured by connecting external devices in partyline fashion as shown in Figure 2-1. The I/O cable contains 8 input data lines, 8 output data lines, 1 input strobe line, 8 (of the 24) external command lines, 1 clock line, and 7 power and ground lines.

4.4 I/O DATA LINES

The data lines are broken into two groups. 8 lines are used for output and 8 lines are used for input.

The data output lines are connected (at all times) to the A-register in the processor and are used to perform three basic functions:

a. To transfer an address to select an external device (including the keyboard, c.r.t. and tape decks);

b. To transfer commands to an addressed device; and

c. To transfer data to an addressed device.

The data input lines are strobed into the A-register upon execution of the INPUT instruction and used to perform two basic functions.

a. To transfer status information from an addressed external device; and

b. To transfer data from an addressed external device.

As shown in Figure 4-1, input data or status from the data input lines is processed through input receivers and gated into the A-register. Once in the A-register data can be manipulated or stored as desired. Addresses, commands, or data that is to be transferred to an external device must first be loaded into the A-register. From the A-register it is transmitted through output devices onto the data output lines. The A-register, then, is used as a buffer register between the 2200 processor and external devices for all input and output data transfers.

4.5 INPUT STROBE

The INPUT STROBE carries a signal (8 usec. pulse) from the processor to the external device to indicate that whatever data is on the data input lines has been sampled and transferred into the A-register. The trailing edge of the pulse may be used by an external device to remove data from the data input line or to clear a status bit. The INPUT strobe is generated upon execution of the INPUT instruction.

4.6 EXTERNAL COMMAND STROBES

The eight EXTERNAL commands usec by devices physically external to the Model 2200 are given function assignments as follows:

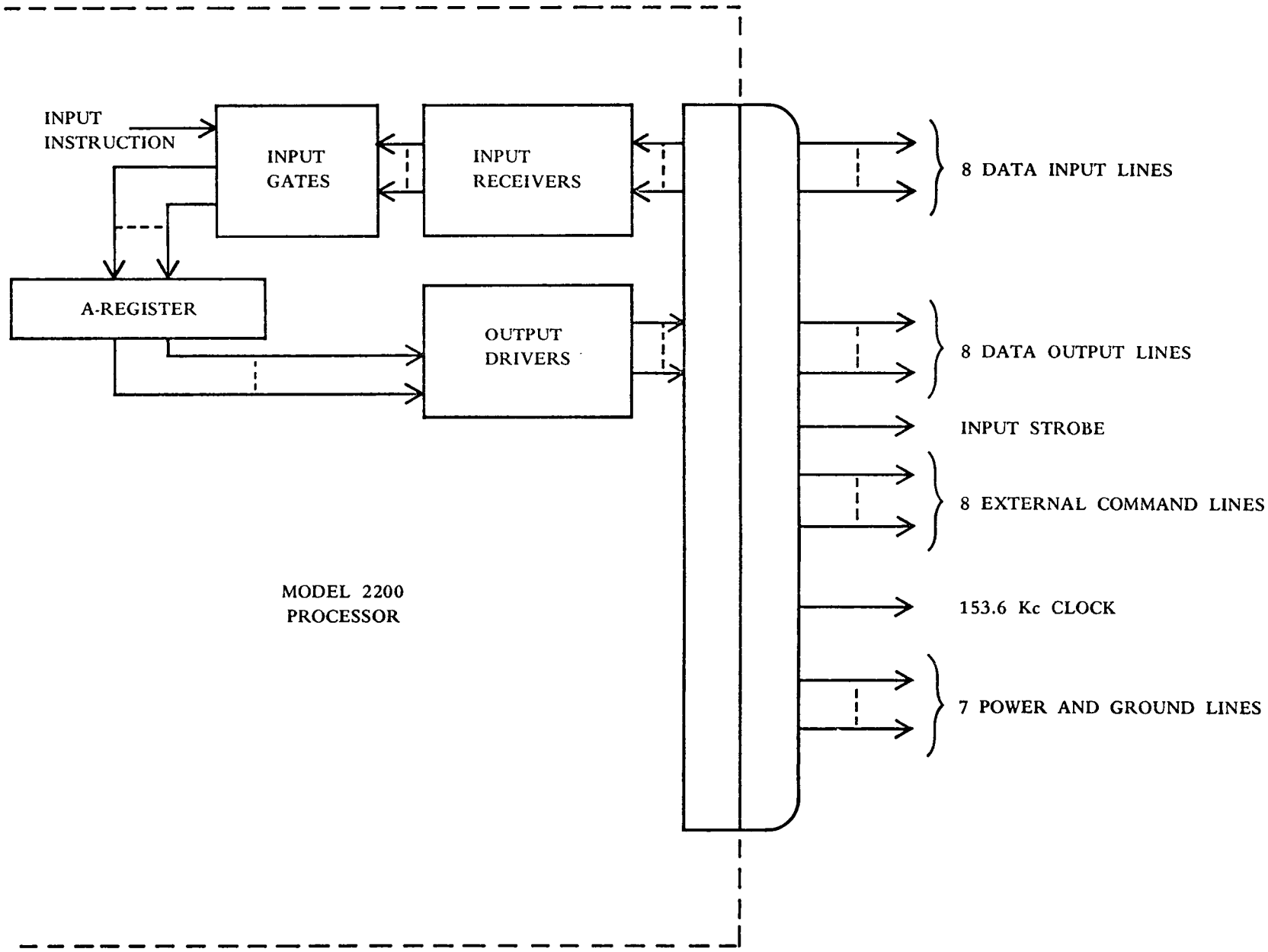


FIGURE 4-1

I/O SYSTEM, FUNCTIONAL DIAGRAM

TABLE 4-1

EXTERNAL COMMANDS

EX (exp)

COMMAND NUMBER	(exp)	OCTAL CODE	COMMAND	DESCRIPTION
1	ADR	121	Address	Selects device specified by A-register
2	STATUS	123	Sense Status	Connects selected device status lines to data input bus
3	DATA	125	Sense Data	Connects selected device data lines to data input bus
4	WRITE	127	Write Strobe	Signals selected device that output data is on data output lines
5	COM1	131	Command 1	Signals selected device that a control word is on data output lines
6	COM2	133	Command 2	Signals selected device that a control word is on data output lines
7	COM3	135	Command 3	Signals selected device that a control word is on data output lines
8	COM4	137	Command 4	Signals selected device that a control word is on data output lines

Execution of an EXTERNAL instruction provides a pulse 8 microseconds long. No functions are performed within the 2200 processor during execution of an EXTERNAL instruction. The interpretation of each of the EXTERNAL instructions is as follows:

a. Address. The address command (EX ADR) is a signal from the processor to all external devices to indicate that the information on the data output bus is to be interpreted as an external device address. Whenever an address command is executed all external devices should be disconnected from the I/O system except the device whose address appears in the A-register. (See paragraph 4.10 for discussion of address assignments).

b. Sense Status. The sense status (EX STATUS) command is a signal from the processor to the selected external device to place status information on the data input lines. (Note: External devices should be configured such that status is connected to the data input line whenever the device is first addressed. It is only necessary to use the EX STATUS instruction when it is desired to sense status after an EX DATA instruction has been used and a new address sequence has not been executed).

c. Sense Data. The sense data (EX DATA) command is a signal from the processor to the selected external device to place its data on the data input lines.

d. Write Strobe. The write strobe (EX WRITE) command is a signal from the processor that data is present on the data output lines for the selected external device.

e. Command 1 through Command 4. Command 1 through Command 4 (EX COM1, etc.) have meaning appropriate to the device selected. Reference should be made to a description of each device for specific function assignments.

4.7 CLOCK LINE

The clock line is crystal controlled 153.6 kilohertz squarewave that is available to external devices for timing purposes.

4.8 I/O BUS ELECTRICAL SPECIFICATIONS

All signals in the I/O System operate with a voltage swing of zero to +5 volts. Line drivers have a source impedance of approximately 470 ohms and line receivers have an input impedance in excess of 18,000 ohms and a decision threshold of +1.7 volts. Figure 4-2 illustrates a typical output line circuit.

All logic levels are True (logical 1) for zero (less than +1.7) volts and False (logical 0) for +5 (greater than 1.7) volts.

4.9 DATA TRANSFER OPERATION

a. Data Output. Figure 4-3 illustrates the sequence of events that occur when data is transferred from the

2200 processor to an external device. A typical program sequence to execute a transfer is as follows:

```
WDATA   LA 0322      Load device address into A-
                     register
        EX ADR
        INPUT        Load device status into A-register
        SRC          Shift desired status bit into C
                     flip-flop
        JFC EXIT     Exit if device not ready
        LAM          Load A-register with DATA
        EX WRITE     Write Data to device
```

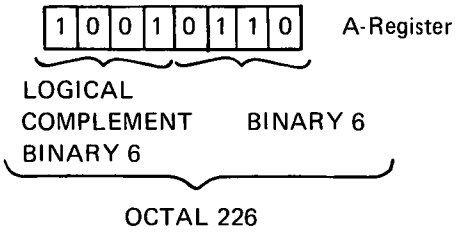
Once a device is addressed it remains addressed until another device is addressed so that succeeding commands may be transmitted to a device without re-addressing the device. Transmitting a command to a device would follow a program sequence similar to a data transfer except that EX COM_n would replace EX WRITE.

b. Data Input. Figure 4-4 illustrates a sequence of events that occur when data is transferred from an external device to the 2200 processor. A typical program sequence is as follows:

```
RDATA   LA 0322      Load A-register with device
                     address
        EX ADR
        INPUT        Load device status into A-register
        SRC          Shift status bit into C flip-flop
        SRC
        JFC EXIT     Exit if device not ready
        EX DATA      Place data on input lines
        INPUT        Load A-register with data
```

4.10 DEVICE ADDRESS NUMBERING

Address assignments in the I/O system provides for up to 16 devices external to the 2200 processor. The address word is formulated such that the low-order four bits form the binary value for the address and the high-order four bits form the logical complement of the low order bits. For example device number 6 would have an address word as follows:



This addressing system permits any device to be coded for its particular address with only a four-input gate strapped to those output lines that are set to one during the address command. In addition, all devices can be cleared by setting the A-register to all zeros and executing an EX ADR instruction.

Device addresses used in the Model 2200 are given in the following table:

TABLE 4-2

DEVICE ADDRESS ASSIGNMENTS

DEVICE	NUMBER	BINARY	OCTAL
Cassette Tape Decks	0	11110000	360
CRT/Keyboard	1	11100001	341
Communications Adaptor	2	11010010	322
2200P Printer	3	11000011	303
2200T Tape Transport	4	10110100	264
Unassigned	5	10100101	245
"	6	10010110	226
"	7	10000111	207
"	8	01111000	170
"	9	01101001	151
"	10	01011010	132
"	11	01001011	113
"	12	00111100	074
"	13	00101101	055
"	14	00011110	036
"	15	00001111	017

4.11 I/O POWER AND GROUND LINES

The Model 2200 provides several power supply voltages for use by external devices. Table 4-3 below lists the characteristics of each power and ground line.

4.12 I/O SYSTEM CONNECTOR

Connection to the I/O system is made through an Amphenol 17-20500-1 connector. The mating I/O cable should have a 50-pin Amphenol 17-10500-1 connector.

Table 5-5 lists the pin assignments.

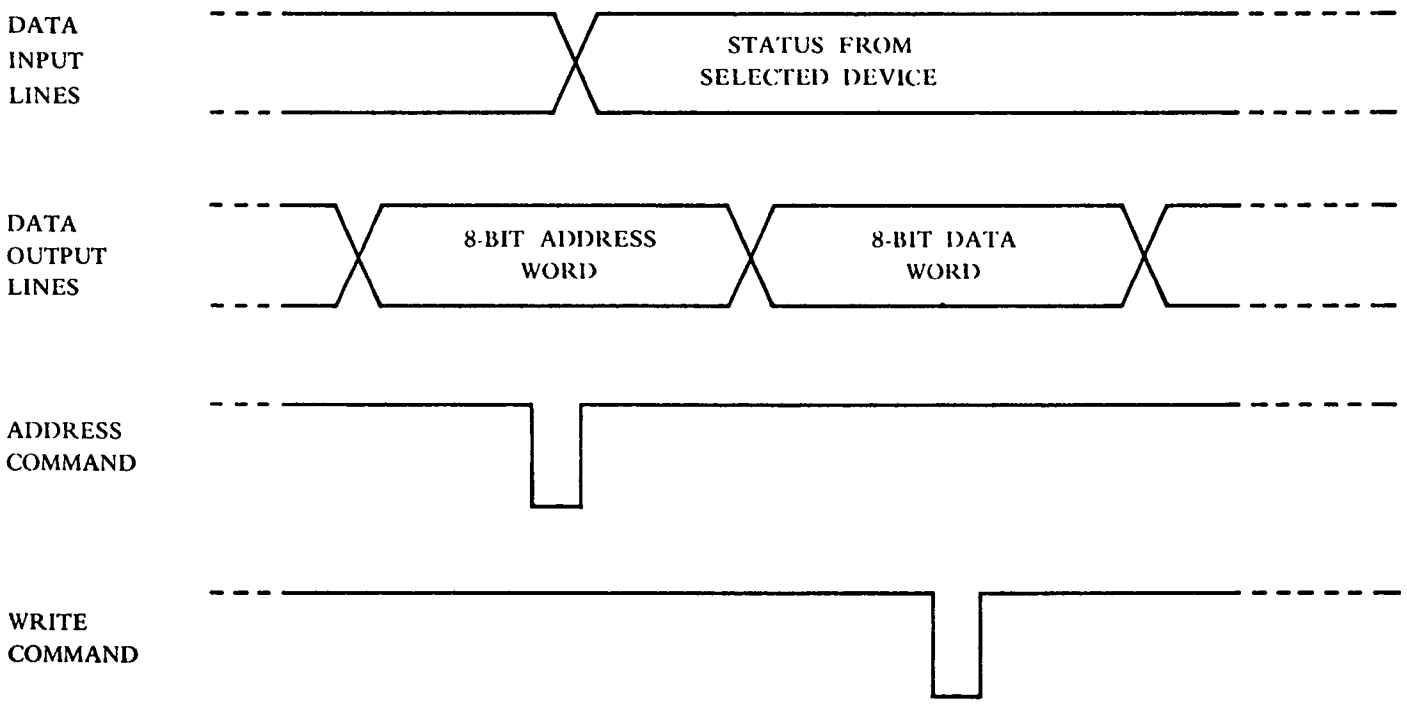


FIGURE 4-3

TYPICAL DATA OUTPUT
SEQUENCE

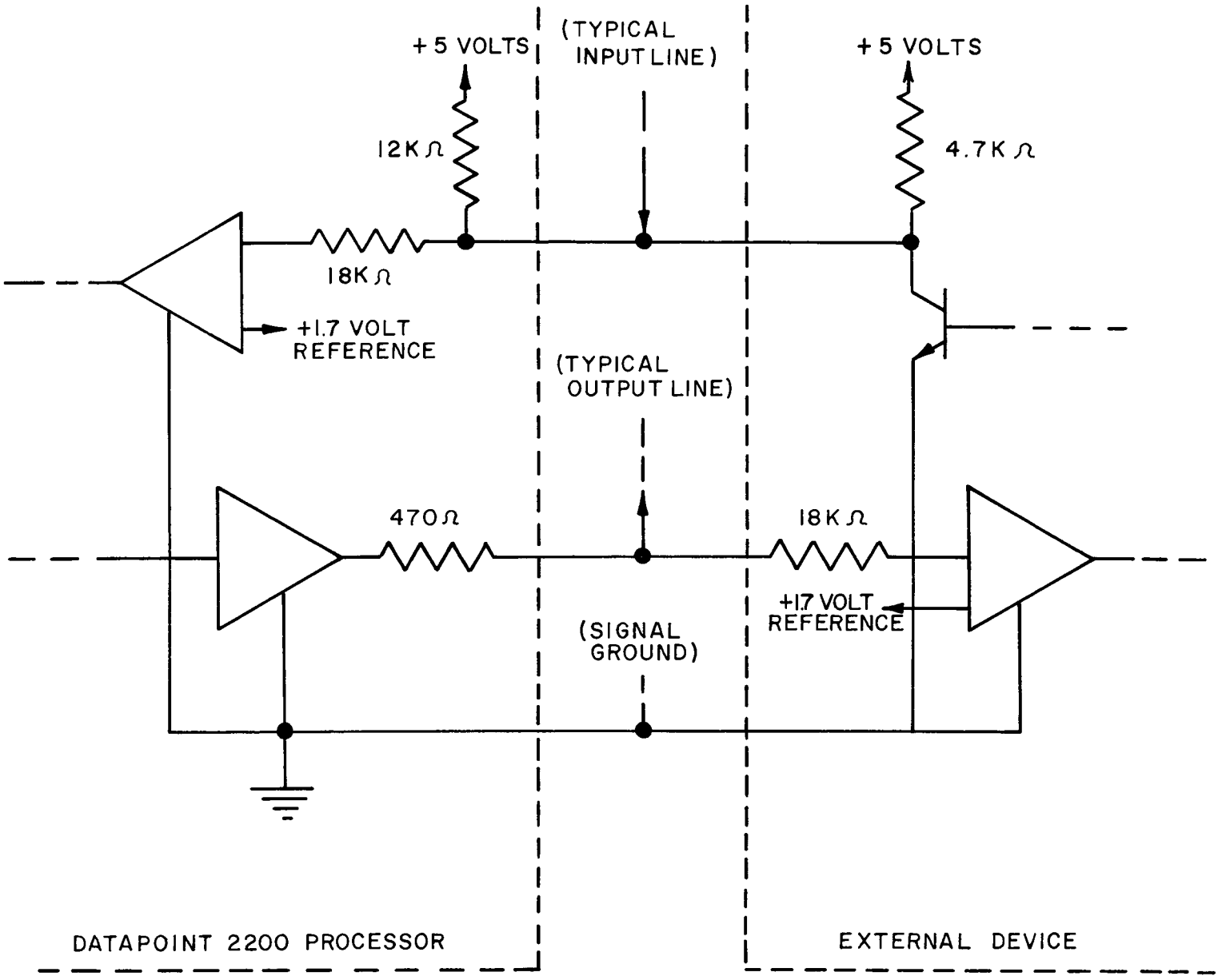


FIGURE 4-2

I/O CABLE, ELECTRICAL CHARACTERISTICS

TABLE 4-3

I/O POWER AND GROUND LINES

VOLTAGE	MAX. CURRENT	REGULATION
-12 Volts	0.5 amps	±10%
- 5 Volts	0.1 amps	±5%
+ 5 Volts	3.4 amps	±5%
+12 Volts	0.5 amps	±10%
+24 Volts	0.1 amps	±5%
Power Ground	–	–
Signal Ground	–	–

TABLE 4-4

I/O CONNECTOR PIN ASSIGNMENTS

ASSIGNMENT		PIN NUMBER
Data output	0	44
	1	45
(A Bus Outputs)	2	46
	3	29
	4	30
	5	31
	6	32
	7	33
Data Input	0	1
	1	2
(A Bus Inputs)	2	3
	3	4
	4	5
	5	6
	6	7
	7	18
Input Strobe (Read)		12
Address Command		15
Sense Status Command		13
Sense Data Command		14
Write Command		19
Command 1		20
Command 2		21
Command 3		22
Command 4		23
153.6 KHz Clock		39
-12v		24
-5v		27
+5v		8, 9, 10, 11
+12v		25
+24v		26
Ground (Power & Signal)		40, 41, 42, 43

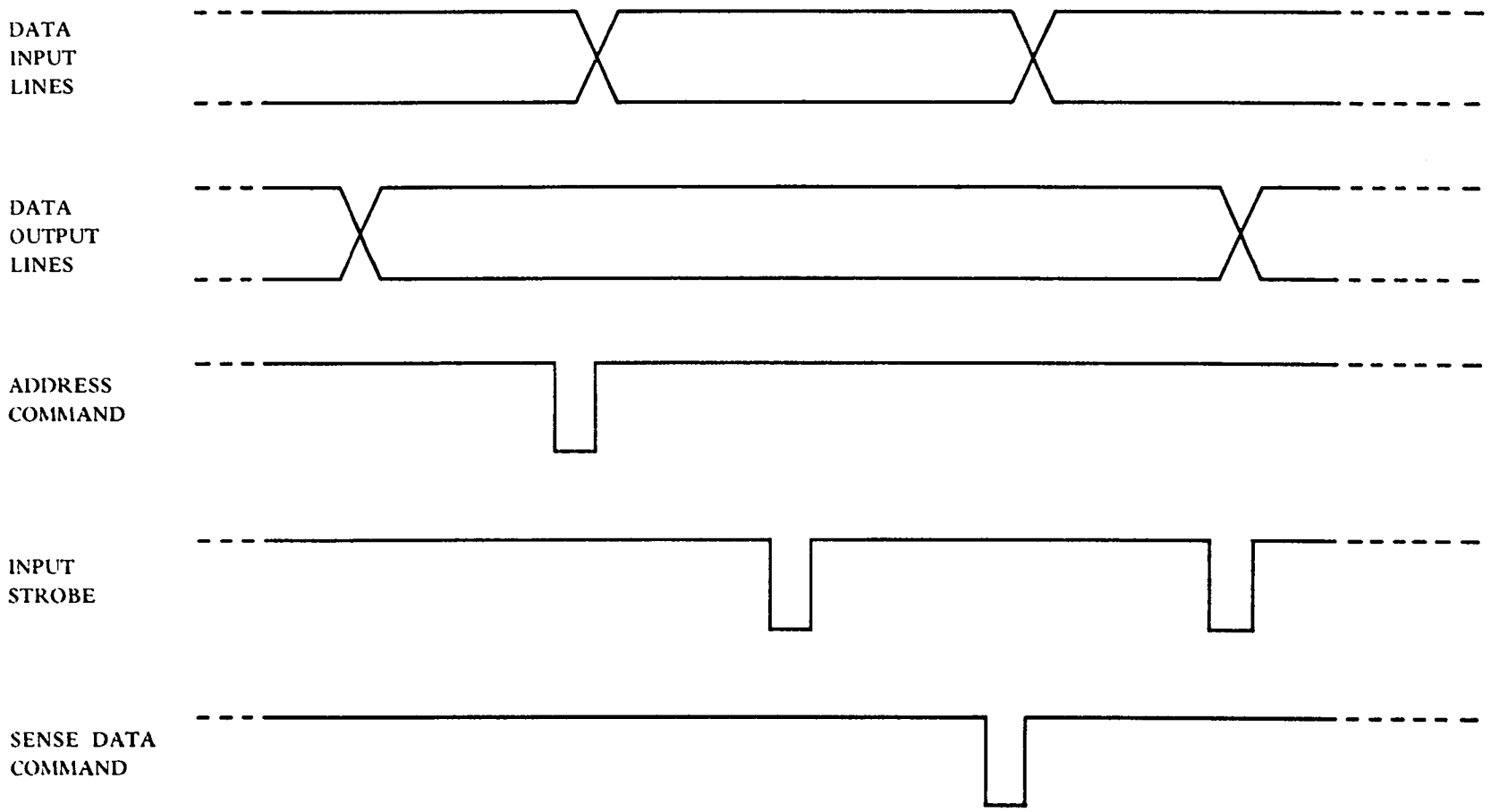


FIGURE 4-4

TYPICAL DATA INPUT
SEQUENCE

PART 5

KEYBOARD

5.1 GENERAL DESCRIPTION

The keyboard on the Datapoint 2200 performs the functions of data entry and processor control. The keys are divided into three sections, each of which has it own function.

Section 1 consists of 41 standard alphabetic, numeric and special character keys found in the ASCII character set. Figure 5-1 illustrates the keyboard layout.

Section 2 consists of an 11 key matrix which is identical to a standard adding machine keyboard with the addition of a decimal point (period). The keys in this section are duplicates of certain keys found in Section 1 and are provided to facilitate entry of large amounts of numeric data.

The keys in Section 3 are special function keys which exert control over the processor. Their names and associated functions are as follows:

RUN — Momentary contact switch, which when depressed, causes the processor to begin execution of the instruction located at the address in memory currently addressed by the program counter.

STOP — Momentary contact switch which, when depressed, causes instruction execution to halt at the completion of the current instruction. Care should be taken when using this switch, because any tape operation which may be in progress will be aborted.

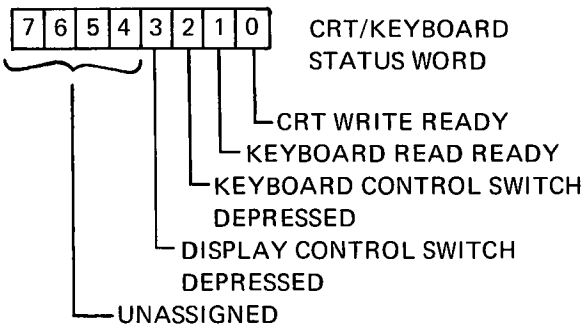
KEYBOARD — Momentary contact switch which sets a status bit that may be tested at any time by the processor.

DISPLAY — Momentary contact switch with a function similar to that of KEYBOARD switch. Either one or both of these switches may be depressed.

RESTART — Momentary contact switch which causes the processor to halt, rewind the system or program tape mounted on Deck 1, load and execute the first record found on tape.

5.2 OPERATION

The keyboard is addressed by the processor by loading the A-register with 341_8 and executing an EX ADR command. (The crt display also uses this address. Data transfers to the processor are from the keyboard and transfers from the processor are to the display). Following the address sequence the c.r.t./keyboard status word can be loaded into the A-register by executing an INPUT instruction. Bit 1 of the A-register may be tested by the program to determine if a character is ready for transfer from the keyboard. Bits 2 and 3 will indicate if either the KEYBOARD or DISPLAY control switch is pressed.



The External Commands associated with the operation of the keyboard are as follows:

a. EX BEEP. This command produces a 1500 Hertz tone for a duration of about 100 msec. The tone could be used as an error or ready signal to the keyboard operator.

b. EX CLICK. This command produces an audible click which could be used to acknowledge receipt of a valid character when a key is depressed.

c. EX COM1 (Command 1). Presents a control word contained in the A-register to the keyboard. Bit 5 of the control word controls the KEYBOARD switch light and bit 6 controls the DISPLAY switch light as follows:

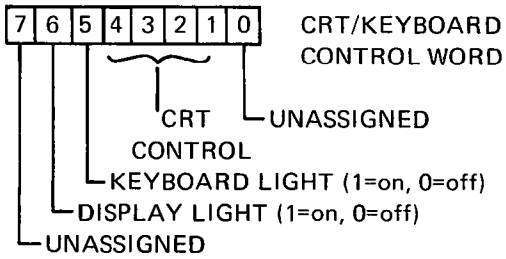


TABLE 5-1

KEYBOARD CODING (ASCII)

A-101	a -141	0-060	: -072
B-102	b -142	1-061	; -073
C-103	c -143	2-062	< -074
D-104	d -144	3-063	= -075
E-105	e -145	4-064	> -076
F-106	f -146	5-065	? -077
G-107	g -147	6-066	[-133
H-110	h -150	7-067	~ -176
I -111	i -151	8-070	] -135
J -112	j -152	9-071	^ -136
		Space-040	_ -137
K-113	k -153		
L-114	l -154	!-041	@ -100
M-115	m-155	"-042	{ -173
N-116	n -156	#-043	\ -134
O-117	o -157	$-044	' -140
P-120	p -160	%-045	| -174
Q-121	q -161	&-046	} -175
R-122	r -162	'-047	Enter-015
S-123	s -163	(-050	Cancel-030
T-124	t -164	)-051	Backspace-010
U-125	u -165	*-052	Rubout (R.O.)-177
V-126	v -166	+-053	
W-127	w-167	,-054	
X-130	x -170	--055	
Y-131	y -171	.-056	
Z-132	z -172	/-057	

PART 6

CRT DISPLAY

6.1 GENERAL DESCRIPTION

The display unit on the Datapoint 2200 consists of a CRT capable of displaying 12 lines of 80 characters each, a character generator, 960 cells of refresh memory (refresh rate 60 Hz), and a group of registers utilized to position the cursor. Maximum character transfer rate to the CRT is 60 characters per second.

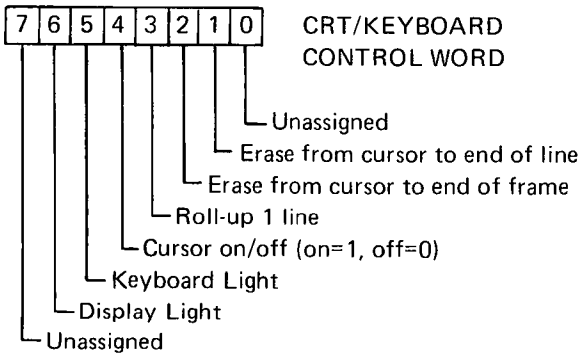
The character set utilized by the CRT display consists of the full ASCII set with both upper and lower case alphabetics and all numeric and special characters.

6.2 OPERATION

The CRT is addressed and status tested in the same manner as the keyboard (see paragraph 5.2). Bit 0 of the status word indicates that the CRT is ready to accept data or commands. Characters are transferred to the screen by loading the A-register with the character to be displayed and executing an EX WRITE. The character will be displayed at the current cursor location.

Control of the CRT is accomplished through the use of the three external commands - Command 1, Command 2, and Command 3. The functions performed by these commands are as follows:

a. EX COM1 (Command 1) Transfers a control word contained in the A-register to the CRT. The applicable bit assignments and their functions are as follows:



The erase functions permit selective erasures on the screen by limiting erasures to those character positions following the current cursor position to the end of the line (or page).

The roll-up function causes all displayed characters (not the cursor) to move up one line. The top line on the screen is lost.

The cursor image may be turned on or off through the control word. The cursor position is the same in either case. The cursor image is automatically turned off whenever the processor is in the HALT state.

b. EX COM2 (Command 2) Positions the cursor to the horizontal character slot designated by the contents of the A-register. Character position $0\text{-}79_{10}(0\text{-}117_8)$ are valid.

c. EX COM3 (Command 3) Positions the cursor to the line designated by the contents of the A-register. Line number $0\text{-}11_{10}$ $(0\text{-}13_8)$ are valid.

In order to write a new character, the cursor must occupy that character's position on the screen. After the character has been written, the cursor should then be moved to the next horizontal (or vertical) position desired. The CRT Write Ready status bit must be true before positioning the cursor or displaying a character.

Both the CRT and keyboard utilize the standard ASCII character set. (See Table 5-1). Any invalid character code will appear as a blank space on the CRT screen.

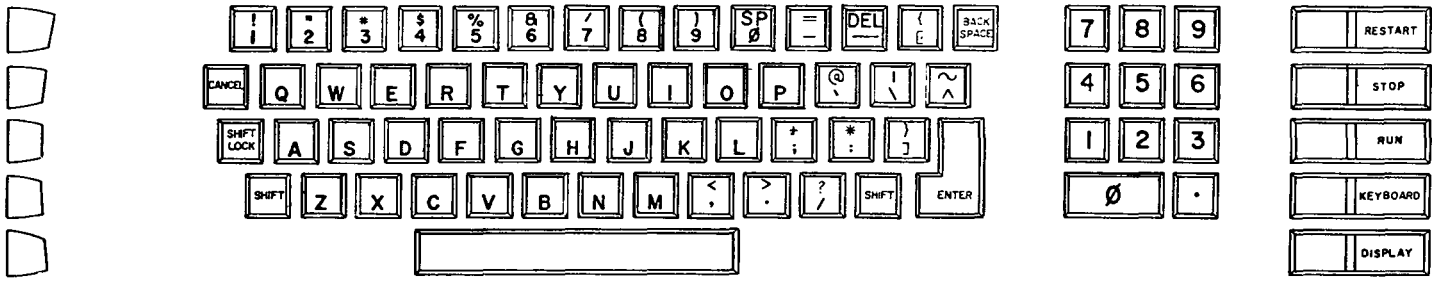


FIGURE 6-1
KEYBOARD LAYOUT

PART 7

CASSETTE TAPES

7.1 GENERAL DESCRIPTION

The Datapoint 2200 contains two cassette tape recording devices for storage of programs and data. Since the hardware RESTART (section 5.1) uses the rear deck (number one), programs will typically be on it while data areas will be the front deck (number two). However, once the machine is initially loaded, either deck may be used for both purposes.

Data on the Tape is organized by record (of any length). Records are written and read at 350 eight-bit characters per second with a tape speed of approximately 7.5 inches per second. See Table 7.1 for a list of the physical specifications.

7.2 OPERATION

Data is recorded or read in bit serial fashion on one track. Each eight bit character is framed by three sync bits on either side of the character:

-	0 1 0	x x x x x x x x	0 1 0	x x x x x x x x	0 1 0	-
	Sync Code	Character 1	Sync Code	Character 2	Sync Code	

The appearance of the correct sync code indicates that the character is valid. Any other sync code causes special action to be taken on data reads. Note that the sync codes are valid for tape motion in either direction so the tape may be read backwards although in the reverse direction the data bits will apear reverse d (bit 0 will be bit 7, 1 will be 6 etc.)

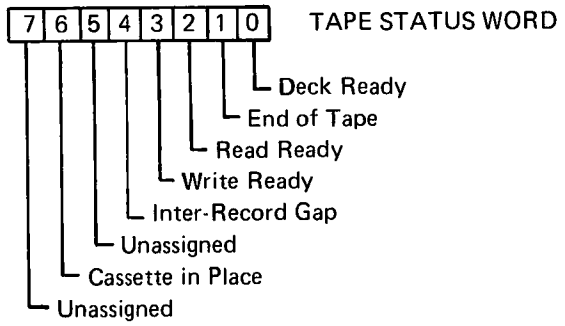
A record is a group of successive valid characters. An inter-record gap is indicated by the failure of the sync code to be zero one zero and all mark code. (ones):

-	0 1 0	x x x x x x x x	0 1 0	x x x x x x x x	1 1 1	x x x	-
	Sync Code	Valid Character	Sync Code	Invalid Character	Sync Code	Inter Record Gap	

Only valid characters will be presented as data from the tape unit.

7.3 STATUS

The cassette tape unit is addressed by the processor by loading the A-register with 360_8 and executing the EX ADR instruction. Following this sequence, the tape unit status can be loaded into the A-register by executing an INPUT instruction. The bit assignments are as follows:



DECK READY	Deck ready will be set whenever the tape unit is ready to accept another command. (Only the TSTOP command should be issued if this bit is false). The tape will be stopped, a cassette in the selected deck and not wound to the clear leader at either end, and the head engaged when this bit is true. This bit should be checked after selecting a deck.
END OF TAPE	End of Tape indicates that the cassette has run onto leader (in either direction).
READ READY	Read Ready indicates that the selected deck has read another character.
WRITE READY	Write Ready indicates that the selected deck is ready to write another character.
INTER-RECORD GAP	Inter-Record Gap indicates the selected deck has come across an inter-record gap (invalid sync code).
CASSETTE IN PLACE	Cassette in Place indicates that a cassette is physically in place in the selected deck.

7.4 CONTROL

When the cassette tape unit is addressed the following instructions will control the action of the tape:

a. EX TSTOP causes any motion of either deck to be stopped, any read or write operations to be terminated. When everything has settled, the ready status bit will come true and operations may be resumed.

b. EX DECK1 causes deck one (rear) to be the currently selected deck. Before commanding a deck selection, care should be taken that the currently selected deck has completed all operations.

c. EX DECK2 causes deck two (front) to be the currently selected deck. Note the precaution in (b).

d. EX RBK causes the currently selected deck to be set in forward motion and, after 70 msec, for the read circuitry to be enabled. The read ready status bit will come true upon appearance on the tape of the first valid character. Upon appearance of an invalid sync code, the inter-record gap status bit comes true and tape motion is automatically stopped. Note that this will happen only after at least one valid character has been found. Once the read ready status bit comes true, the character must be taken within 2.8 milliseconds or it will be overwritten with the next one. The tape read hardware double-buffers incoming characters to allow the 2.8 msec character availability.

e. EX BSP is similar to EX RBK except that tape motion is in the reverse direction so the data bits will be reversed.

f. EX SF is similar to EX RBK except the tape is not stopped upon appearance of an inter-record gap, and if allowed to continue will start to read the next record on the tape. In this case, the read ready status bit will come true again after the first character of the next record is read. Only an EX TSTOP will stop the motion initiated by EX SF.

g. EX WBK causes the currently selected deck to be set in forward motion and for all status bits except the write ready to go false. A character must then be presented within 2.8 milliseconds (the first character will be accepted at once due to the buffering in the tape hardware and then there will be a pause while the tape comes up to speed), at which time the write ready will go false until the writing circuitry is ready to accept another character. An end of record is a signalled to the hardware by withholding a character for a period of time longer than 2.8 milliseconds specified above. When this is done, the write ready will go false, an inter-record gap will be written, the tape motion will cease, and the deck ready status bit will come true again.

h. EX REWIND causes the tape to be rewound to the beginning on the selected deck. Worst case rewind time is approximately 40 seconds.

i. PUNCH TABS, on the Cassette Cartridge are used for "write protect" and "automatic restart". The punch tab on the left (as you face the terminal) inhibits the ability to write on tape, when punched. When the tab on the right is punched, it causes an automatic restart whenever a halt or power-up occurs.

TABLE 7-1

TAPE UNIT PHYSICAL SPECIFICATIONS

Density	47 characters/inch
Speed	7.5 ips
Recording Rate	350 c.p.s.
Capacity	130,000 characters (typical)
Start/Stop Time (Inter-Record Gap)	280 msec.
Start/Stop Distance (Inter-Recrod Gap)	2 inches
Rewind Speed	90 ips
Rewind Time (max 300 ft.)	40 sec.
Character Transfer Time	2.8 msec.

PART 8

COMMUNICATIONS ADAPTOR

8.1 GENERAL DESCRIPTION

The 2200 Communications Adaptor is an external device, which when connected to the Datapoint 2200 Input/Output System permits asysnchronous serial data interchange to other remote systems or devices.

The Communications Adaptor consists of three basic parts:

a. The serial data transmitter and time base;

b. The serial data receiver and time base; and

c. The communications channel interface.

The communications channel interface may be one of four types:

a. An EIA RS-232 type interface;

b. An isolated high-level neutral or polar telegraph loop interface;

c. A modem compatible with the Bell System 103 type modems;

d. A modem compatibel with the Bell System 202 type modems.

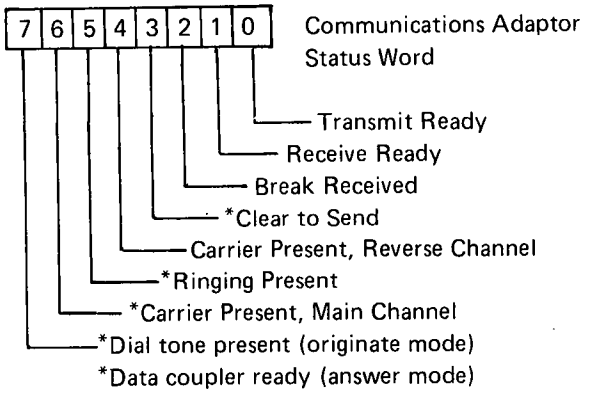
8.2 OPERATION

The serial data transmitter and receiver are addressed at the same time (the address of the first used communications adaptor is 322_8 - see Table 4-2). Additional adaptors may be given previously unassigned addresses.

To set the bit rate desired for the transmitter time base two successive EX COM3 instructions are used to transfer two 8-bit masks from the A-register (See paragraph 8.6 for a discussion of time base mask words). For the receiver EX COM2 is used.

To set the character length for the transmitter and receiver an EX COM4 command is executed with a character length mask from the A-register (see paragraph 8.7 for a discussion of character length mask words).

The status of the communications adaptor is transmitted to the A-register with the following bit assignments:



*Used with data set options.

Communications Adaptor Status Bit Description

Bit 0, Transmit Ready

The "true" condition of this bit indicates that the serial transmitter is ready to accept a new character for transmission. Should another write command be issued to the Communications Adaptor while this bit is "false", i.e. transmitter NOT ready, the previous character will be written over.

Bit 1, Receiver Ready

The Receive Ready bit, in the true state, indicates the presence of a new received character. A read command to the Communications Adaptor returns this bit to the false state. If a read command is not issued before another new character is received, the new character will replace the existing character and the status will remain true.

Bit 2, Break Received

The Break Received status bit simply indicates that the received data is in the "space" or "zero" condition for longer than one character time.

Bit 3, Clear to Send

The true state of Clear to Send status indicates that the data set (internal or external) is prepared to accept data for transmission. This bit has meaning only when an internal or external data set is in used.

Bit 4, Carrier Present - Reverse Channel

This status bit has significance only when operating half-duplex with either an internal or external 202 type data set (modem). The true condition indicates that the reverse (supervisory) channel carrier is being received.

Bit 5, Ringing Present

The true condition of Ringing Present indicates that the ringing of an incoming call has been detected. This bit has significance only when used with an internal or external (with proper options) data set.

Bit 6, Carrier Present - Main Channel

The true condition of this status bit indicates that the main channel carrier is being received. This status bit has meaning only when used with an internal or external data set.

Bit 7, (1) Data Tone Present (Originate Mode)
(2) Data Coupler Ready (Answer Mode)

(1) When originating a call, the true condition of this status bit indicates that a dial tone is present and dialing may proceed; during dialing, the status will become false. Following dialing, and a 2 to 5 second delay, this bit will return to the true condition indicating connection to the telecommunication network (but does not indicate the called number has answered).

(2) When answering a call, the true condition of this status bit indicates that the data coupler is connected to the telecommunications network.

8.3 DATA OUTPUT

After addressing the communications adaptor transmission of each character is accomplished in the following manner:

a. Input the status word and verify that status bit 0, Transmit Ready, is set to 1 indicating that the adaptor can accept another character.

b. Load the A-register with the byte to be transmitted.

c. Apply a write strobe (EX WRITE). Data present on the A-bus will be loaded into the data transmitter and data will be serially transmitted at the selected code length and bit rate.

8.4 DATA INPUT

After addressing the communications adaptor, reception of each character is accomplished in the following manner:

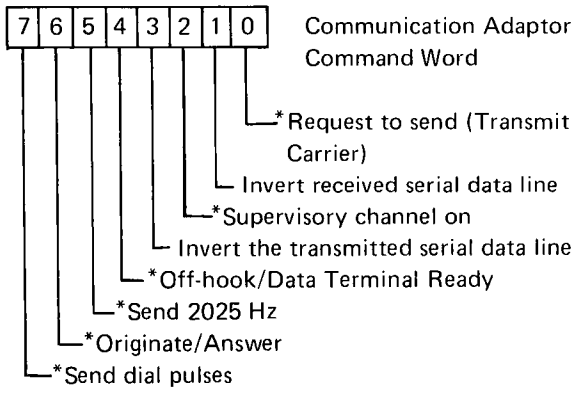
a. Input the status word and verify that status bit 1, Receiver Ready, is set to 1, indicating that a character has been received.

b. Execute an EX DATA instruction.

c. Execute an INPUT command, transferring the received character to the A-register.

8.5 COMMAND WORD

Control of the communications adaptor is accomplished through the use of a command word. The command word is transmitted to the adaptor by executing EX COM1.



*Used with data set options

Communication Adaptor Command Word Description

Bit 0 - Request to Send

This command bit controls the transmit carrier of an internal or external data set. A "one" in this position turns on the transmit carrier and indicates to the data set that it must prepare for data transmission.

Bit 1 - Invert Received Serial Data Line

A "one" in this position permits data to be received normally when the received serial data line is inverted.

Bit 2 - Supervisory Channel On

This command is used only with a 202 type modem in half-duplex operation. A "one" in this command indicates to the modem that the supervisory (or reverse) channel will be operative, transmit or receive.

Bit 3 - Invert Transmitted Serial Data

A "one" in this command inverts the transmitted serial data.

Bit 5 - Off-Hook

A "one" must be placed in this bit position any time a telecommunication call is to be originated or answered. This command allows connection to be made to the telecommunication network with an internal modem and a Bell System Data Access Arrangement. When using an external modem, this command provides "Data Terminal Ready" to the external modem, i.e., the system is prepared for on-line communications. This command is used only for the cases described above.

Bit 5 - Send 2025

This command is used only with an internal 202 type modem, half-duplex operation and "answer" mode. The only use of this command is described as follows:

1.) following receipt of Ringing Present, Status Bit 5, the Off Hook Command, Command Bit 4, is set to a "one".

2.) Next, Status Bit 7, Data Coupler Ready must become "true".

3.) Send 2025 command must now be set to a "one" only for a period of 1/2 second to 3 seconds to inform the calling data set of our response.

Bit 6 - Originate

This command is used only with internal data sets (modems). A "one" in this command instructs the modem that the system will originate a telecommunication call, A "zero" tells the modem the system is prepared to answer a telecommunication call.

Bit 7 - Send Dial Pulses

This command is used only with internal data sets (modems) and is set to "one" only when dialing. Its use is described as follows:

1.) Off-Hook Command (Bit 4) is set to "one".

2.) Status Bit 7 - Dial Tone Present becomes "true".

3.) Bit 7, Bit 4 and Bit 3 (invert xmit), are now set to "one".

4.) When the last dial pulse is completely transmitted, Bit 7 and Bit 3 must be returned to "zero".

One additional command bit, Bit 6 (output control) of the Character Length Mask Word, is used to control the EIA RS-232 Transmitted Data and the High-Level Keyer Transmitted Data. A "one" in this command bit enables serial data to be transmitted only to the EIA RS-232 output or to the High Level Keyer. A "zero" in this command bit allows serial data to be transmitted only to an internal data set (modem).

8.6 TIME BASE MASK WORDS

Both time base generators are programmed for their respective bit rates by the processor. Each time base is independently controlled to allow transmission and reception at different rates.

After addressing the communication interface, two eight-bit mask words are loaded into the time base registers to synthesize the selected bit rates. As each respective byte is presented, a corresponding EX COM2 instruction must be executed to load the receive time base and an EX COM3 instruction to load the transmit time base.

These two bytes are combined to form a 16 bit word which is placed in a holding register. A counter is then set to the value in the holding register. This counter is incremented at the rate of 153,600 Hz. Each time the counter overflows, i.e., goes from all one to all zeroes, a pulse is generated and the counter is reset to the value in the holding register. The time between pulses represents 1/2 clock period or 1/2 bit time. Given a bit rate (bps), the following formula can be used to determine the number N to be entered into the holding register:

$$N = 65{,}536 - \left(\frac{76{,}800}{bps}\right)$$

This number N may then be converted to a 16 bit binary number and separated into the two 8-bit mask words.

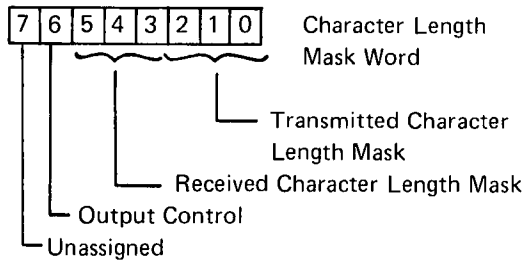
The octal codes for some of the more frequently used rates are listed below:

BIT RATE	1ST MASK WORD	2ND MASK WORD
1) 100*	374	377
2) 110	375	106
3) 220	376	243
4) 440	377	121
5) 150	376	000
6) 300	377	000
7) 600	377	200
8) 1200	377	300
9) 2400	377	340
10) 4800	377	360
11) 9600	377	370

*(Dialing)

8.7 CHARACTER LENGTHS

Character lengths for the transmit and receive sections and its output control bit are determined by a character length mask word which is transmitted to the communications adaptor with an EX COM4 instruction.



The functions of the mask bits are given in the following tables:

TABLE 8-1

TRANSMITTED CHARACTER LENGTH MASK BITS

MASK BIT POSITION 210	START UNITS	INFORMATION UNITS	STOP UNITS	CODE BIT POSITIONS 76543210
000	1	8	1	87654321
001	1	8	2	87654321
010	1	7	1	7654321
011	1	6	1	654321
100	1	5	1	54321
101	–	–	–	––
110	–	–	–	––
111	–	–	–	––

When codes having 5, 6, or 7 information units are to be transmitted, the remaining high-order bits in the character byte must be coded to "1".

When a two-unit stop pulse is required for characters having 5, 6, or 7 information bits, the next larger character length is used; the remaining high-order bits (all coded 1) form the stop pulses.

TABLE 8-2

RECEIVED CHARACTER LENGTH MASK BITS

MASK BIT POSITION 543	START UNITS	INFORMATION UNITS	STOP UNITS	CODE BIT POSITIONS 76543210
000	1	8	1 or more	87654321
001	1	8	1 or more	87654321
010	1	7	1 or more	7654321x
011	1	6	1 or more	654321xx
100	1	5	1 or more	54321xxx
101	–	–	–	––
110	–	–	–	––
111	–	–	–	––

When received characters contain 5, 6 or 7 information bits, the remaining low-order bits (as shown above) must be disregarded.

8.8 INTERFACE CONNECTOR

This interface is provided through an Amphenol 17-10500-1 connector. Pin assignements are as follows:

LEAD	FUNCTION	INPUT/OUTPUT
1	Protective Ground	————
2	Protective Ground	————
3	OH (Off Hook)	Output
4	+25v	————
5	DA (Transmission Path Request)	Output
6	R (Ring Indicator)	Input
7	CCT (Data Coupler Ready)	Input
9	DT (4 wire)	Direct
10	DT (2 wire)	Private
11	DR (2 wire)	Line
12	DR (4 wire)	Connection
23	Clear to Send (RS-232)	Input
24	Transmitted Data (RS-232)	Output
28	Signal Ground	————
29	Signal Ground	————
32	+5v	————
33	+5v	————
40	Request to Send (RS-232)	Output
41	Received Data (RS-232)	Input
42	Data Terminal Ready (RS-232)	Output
44	Supervisory Transmitted Data (RS-232)	Output
45	Data Carrier Detector (RS-232)	Input
46	Supervisory Received Data (RS-232)	Input
49	Clock for 3300P	Output
50	Transmit Bit Rate Clock	Output

8.9 HIGH LEVEL OPTION

Interface with telegraph-type current loops is provided with the high level option. This option provides for completely isolated electronic neutral/polar output relay and a completely isolated neutral/polar input relay. Loop voltage may be as high as 400 volts across the relay and as high as 1000 with respect to ground.

Loop resistance and power is not included with the option.

For further information, refer to the Datapoint 2200 Installation Manual.

8.10 103-DATA SET OPTION CHARACTERISTICS

The 103-Data Set option provides for full duplex data transmission for rates up to 300 bits per second with a signalling system that is compatible with the Bell System 103 series Dataphones. Connection to the common carrier lines would normally be made through a Bell System Access Arrangement type F-58118, CBT, or 1001B. Other connections are also possible where automatic dialing or answering is not required.

The data set may be placed in either the answer mode or originator mode through the use of bit 6 of the communications adaptor command word (see paragraph 8.5). Bit 6 is set to 0 for answer mode and 1 for originator mode. The request to send command bit (bit 0) is normally set to 1 with the 103 option to maintain the transmit carrier on.

Operation of the automatic dialing and answering features discussed in paragraph 8.12 and 8.13.

Table 8-3 provides a summary of characteristics of the 103 Data Set option.

TABLE 8-3

103 DATA SET OPTION CHARACTERISTICS

Originate Mode Carrier Frequencies:	Transmit:	Mark: 1270 Hz Space: 1070 Hz
	Receive:	Mark: 2225 Hz Space: 2025 Hz
Answer Mode Carrier Frequencies:	Transmit:	Mark: 2225 Hz Space: 2025 Hz
		Mark: 1270 Hz Space: 1070 Hz
Keying Rate:	Up to 300 bits per second	
Transmit Level:	0 to -10 dbm.	
Impedance:	600 ohms nominal	
Receive Sensitivity:	+5 to -30 dbm.	

8.11 202-DATA SET OPTION

The 202 Data Set option provides for either full or half duplex data transmission for rates up to 1200 bits per second (1800 bits per second on conditioned private lines). This option is compatible with Bell System 202 series Dataphones (including supervisory channel operation) and in addition provides a 150 bit per second supervisory channel when used with another Datapoint 2200 Data Set option of the same type. Connection may be directly to private lines or to common carrier lines through a Bell System Access Assignment type F-58118, CBT, or 1001B where access to the telephone switched network is desired.

Operation of the automatic dialing and answering are discussed in paragraphs 8.12 and 8.13 respectively.

Table 8-4 provides a summary of characteristics of the 202 Data Set option.

TABLE 8-4

202 DATA SET OPTION CHARACTERISTICS

Main Channel Frequencies:	Mark: 1200 Hz Space: 2200 Hz Soft Turn-Off: 880 Hz
Supervisory Channel Frequencies:	Mark: 387 Hz Space: 470 Hz Soft Turn-Off: 330 Hz
Special Command Frequency:	2025 Hz
Main Channel Keying Rate:	Up to 1200 baud (1800 baud on conditioned private lines.)
Supervisory Channel Keying Rate:	Up to 150 baud
Transmit Level:	0 to -10 dbm
Impedance:	600 ohms nominal
Receive Sensitivity:	+5 to -30 dbm

8.12 AUTOMATIC DIALING OPERATION

When using the Datapoint 103 or 202 data set options with the Bell System Access Arrangement type F-58118, CBT, or 1001B it is possible to automatically originate a call into the telephone switches network. The procedure for this function is as follows:

a. Set bits 4 and 6 of the communications adaptor command word to 1 to provide an off-hook signal to the telephone network and to prepare the modem for originate operation.

b. Test bit 7 of the communications adaptor status word for a 1 indicating dial tone present.

c. Set the transmitter time base to 100 bits per second (see paragraph 8.6).

d. Set the character length mask word to all zeros (ten bit length-see paragraph 8.7).

e. Set bits 3 and 7 of the command word to 1 thus inverting the serial transmitter output and transferring this output to the dial pulse keyer.

f. Sequentially transmit the octal byte 360 for each dial pulse required for each number (see paragraph 8.3-Data Output).

g. Program approximately 1 second delay between each number and at the end of the last number transmitted.

h. Re-establish the correct code length and bit rate for data transmission and set command word bits 3 and 7 to zero to restore the normal transmitter output.

8.13 AUTOMATIC ANSWERING OPERATION

When using the Datapoint 103 or 202 data set options with the Bell System Access Arrangement type F-58118, CBT, or 1001B it is possible to automatically answer a call from the telephone switched network.

Ringing is detected simply by testing bit 5 of the Communications Adaptor Status Word, Response to ringing would be to set bit 4 of the Communications Adaptor Command Word to 1 to provide an off-hook signal to the telephone network.

If the 103 Option is used Command Word bit 0 is set to 1 and bit 6 is set to 0 turning on the transmit carrier and selecting the answer-mode carrier frequencies.

If the 202 Option is used bit 5 of the command word is set to 1 for 1/2 to 3 seconds to transmit a 2025 Hz tone to disable echo suppressors and to inform the calling data set of out sequence in the telephone network, after which normal data transmissions occurs.