SYSTEM DEFINITION OF A MOS LSI MICROPROCESSOR

13 MAY 1970

Prepared For

COMPUTER TERMINAL CORPORATION

9725 DATA POINT DRIVE

SAN ANTONIO, TEXAS

78228

TEXAS INSTRUMENTS INCORPORATED

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HOUSTON, TEXAS 77006

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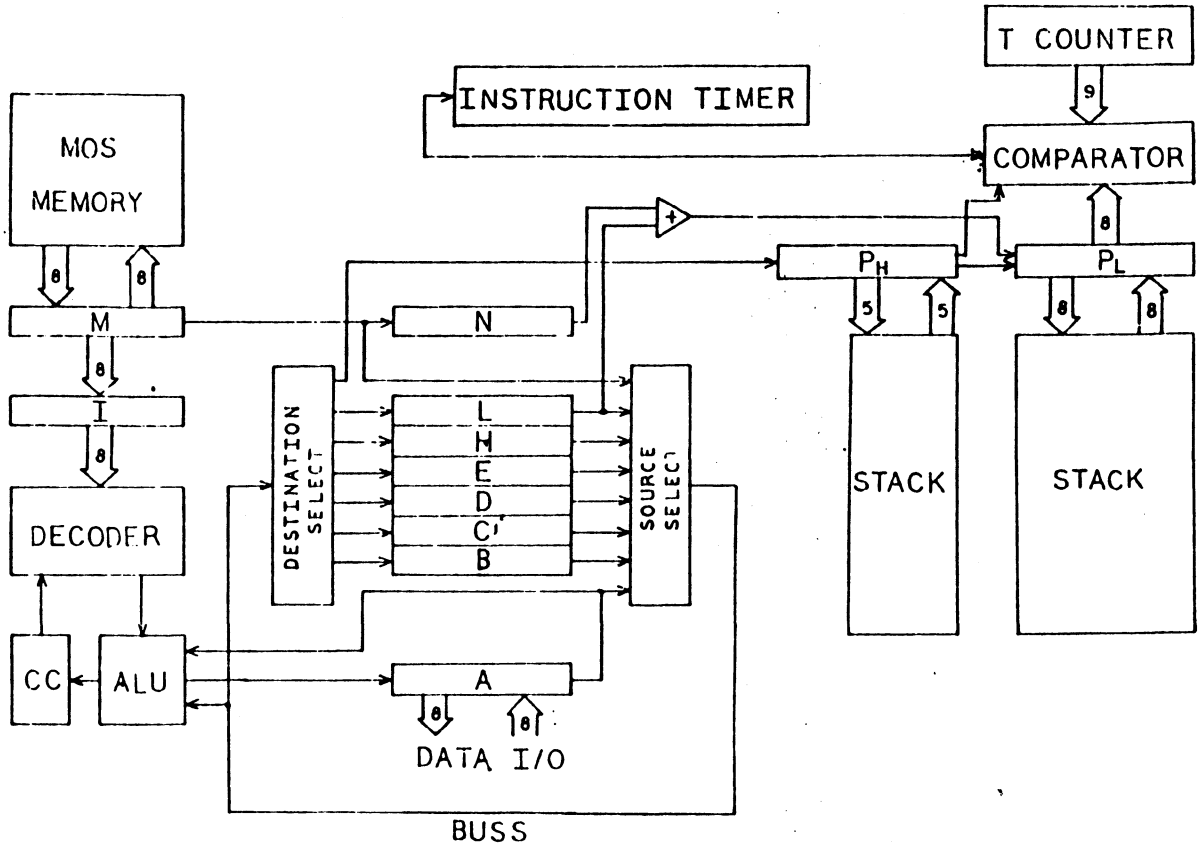
INTRODUCTION

This report serves to define the system organization of an MOS/LSI Computer Processor. This system definition represents the first phase of a three part program to develop and manufacture MOS/LSI circuits for the CTC Data Point 2200 Business Terminal. The primary considerations of the system design is to utilize techniques ideally suited to MOS to design a low cost microprocessor within the performance limits set by CTC. During the system design, critical timing paths were defined and various logic and circuit techniques were evaluated in order to optimize the system performance. As a result, much of the logic and MOS design of phases two and three has been completed so that complications in the latter phases may be minimized.



MATERIAL

FINISH

DRAFTSMAN DATE 5/13/70

DESIGNER DATE

CHECKED DATE

ENGINEER DATE W.J.M.

APPROVED DATE

RELEASED DATE

TEXAS INSTRUMENTS INCORPORATED COMPONENTS GROUP

DWG NO. 01295

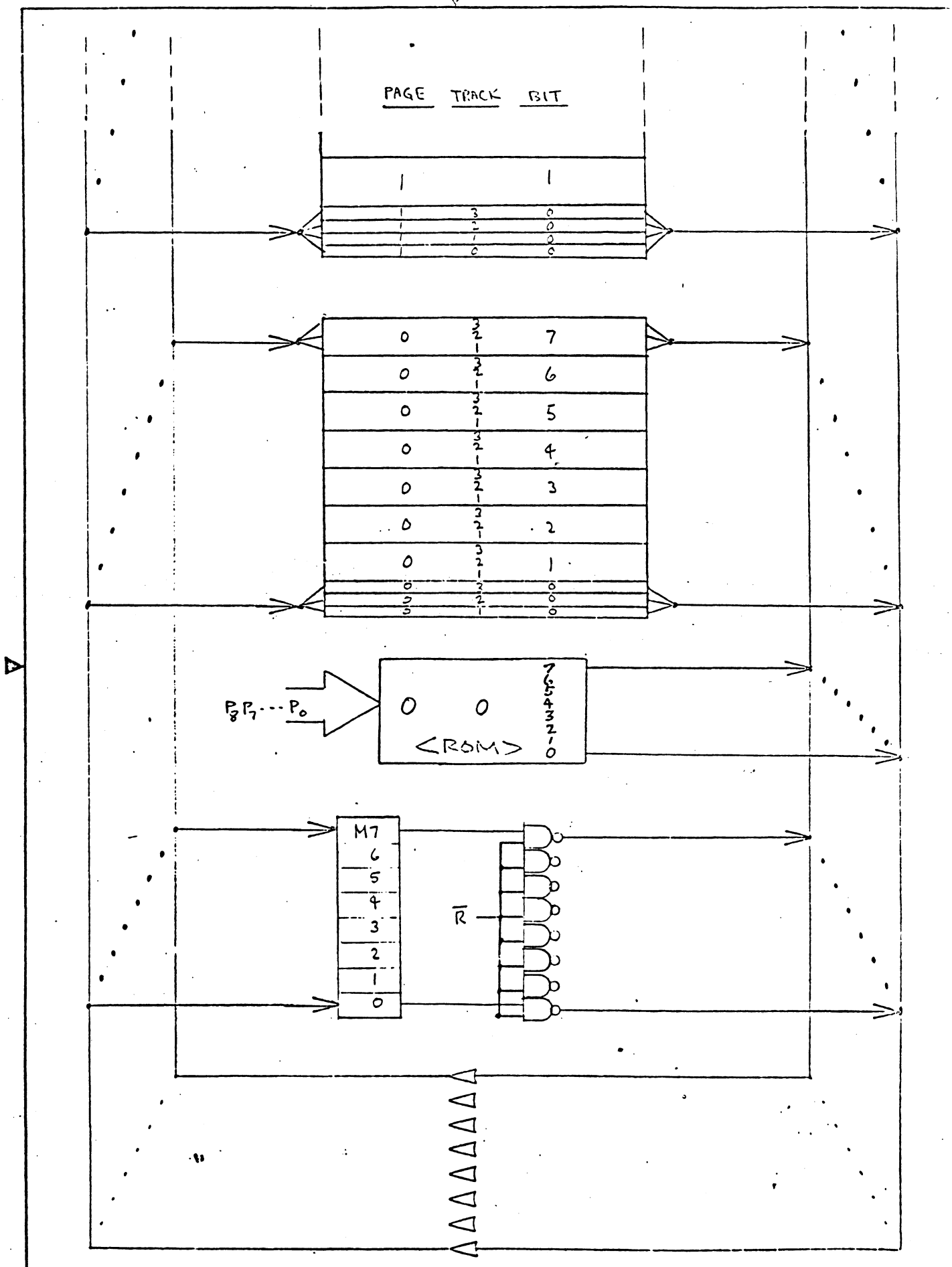
TITLE

SYSTEM BLOCK DIAGRAM

CTC DP 2200

SCALE

B SIZE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0 3 2 1 0
P8 P7 --- P0
0 0
7 6 5 4 3 2 1 0
<ROM>
M7
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5
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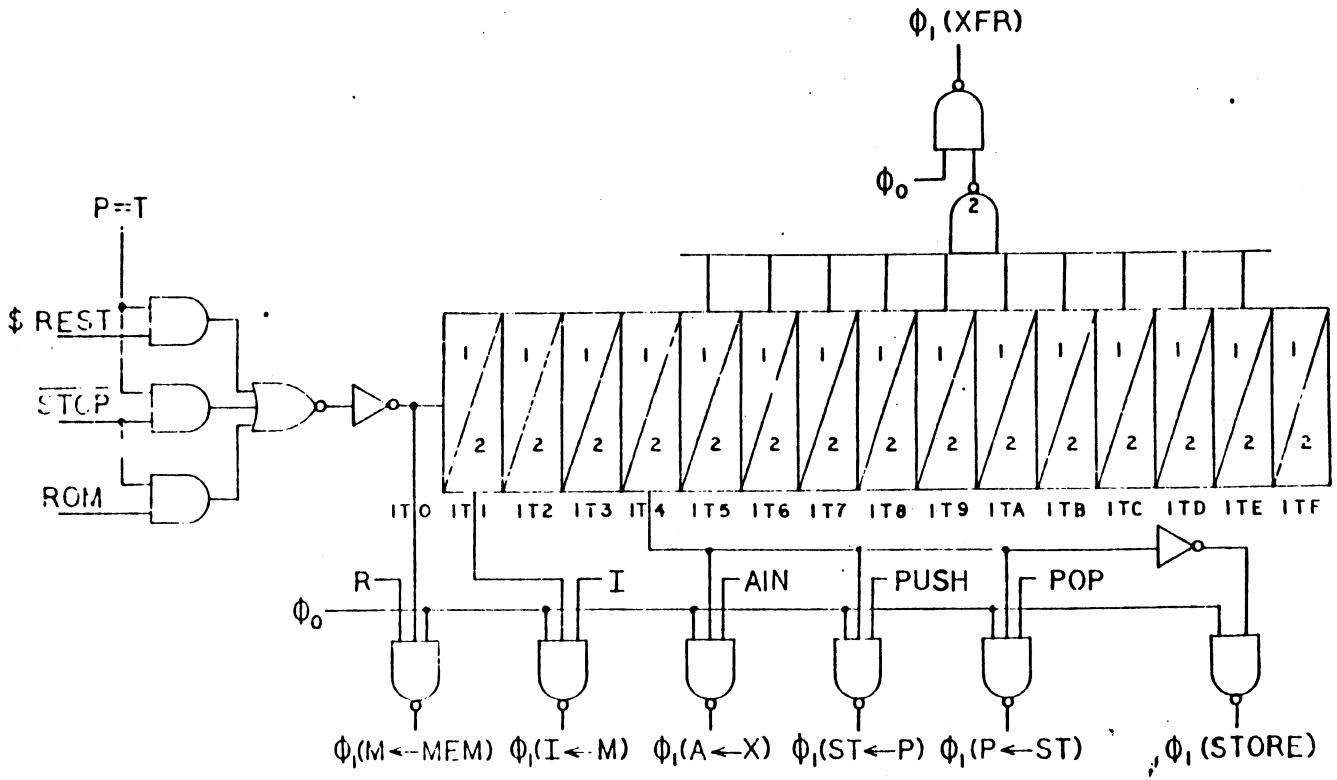
2
1
0
R



MATERIAL

FINISH

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DRAWING NUMBER 01295

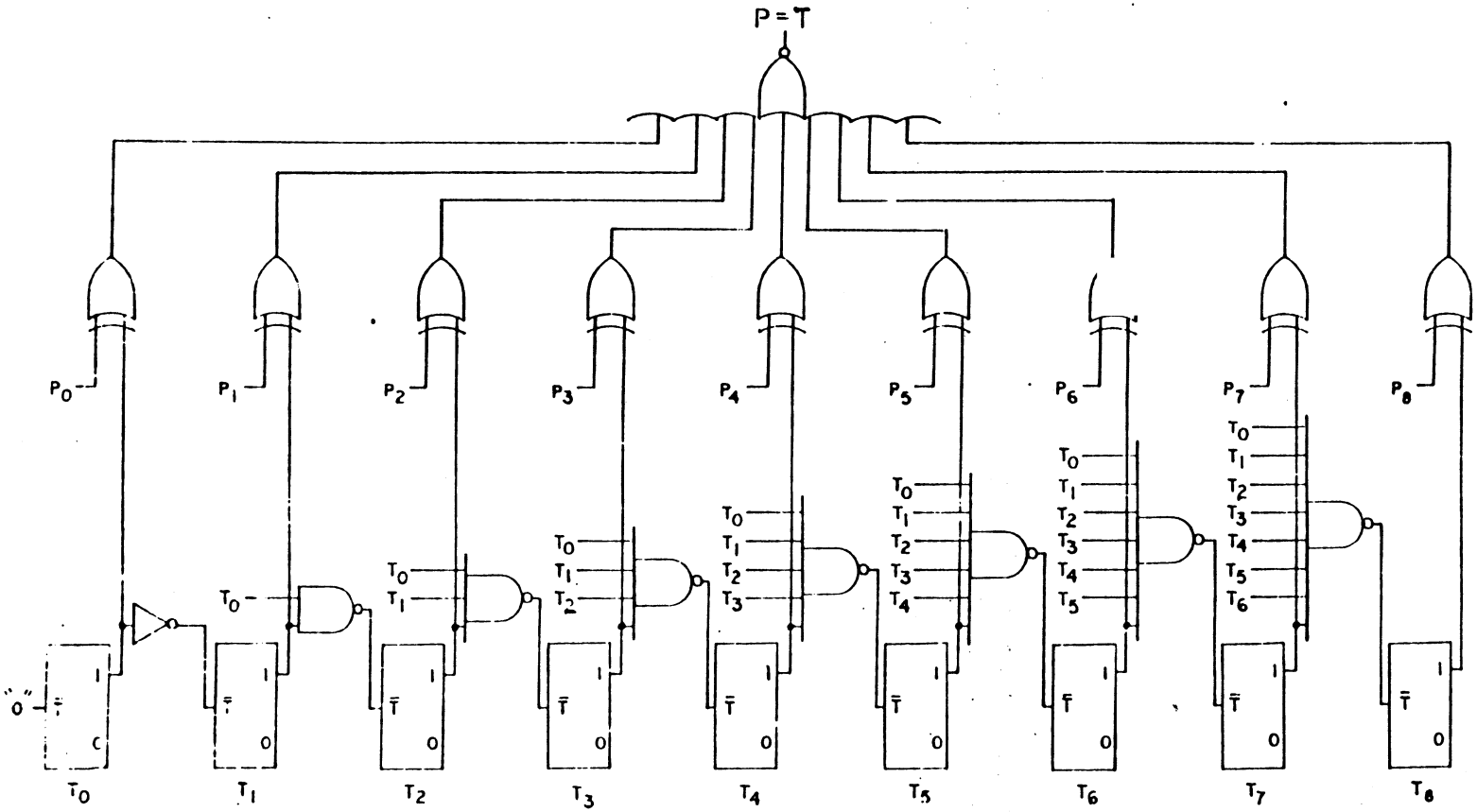
TITLE

INSTRUCTION TIMER

CTC DP2200

SCALE B SIZE

PROPRIETARY



MATERIAL	
FINISH	
DRAFTSMAN	DATE 5/13/70
DESIGNER	DATE
CHECKER	DATE
ENGINEER	DATE
APPROVED W.J.M.	DATE
RELEASED	DATE

TEXAS INSTRUMENTS INCORPORATED
COMPONENTS GROUP

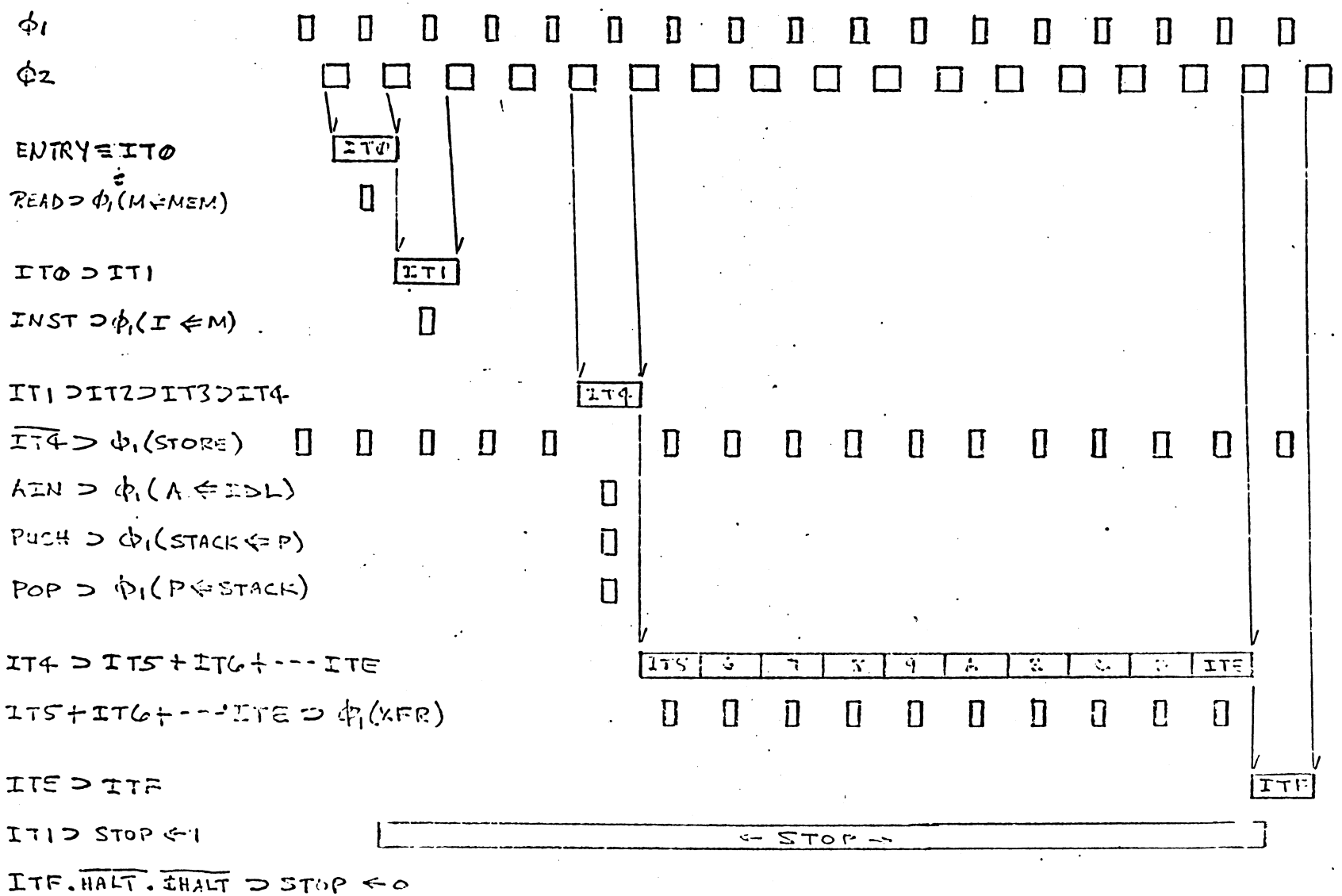
01295

TITLE

T COUNTER & COMPARATOR

CTC DP2200

SCALE | B SIZE | PROPRIETARY INFORMATION

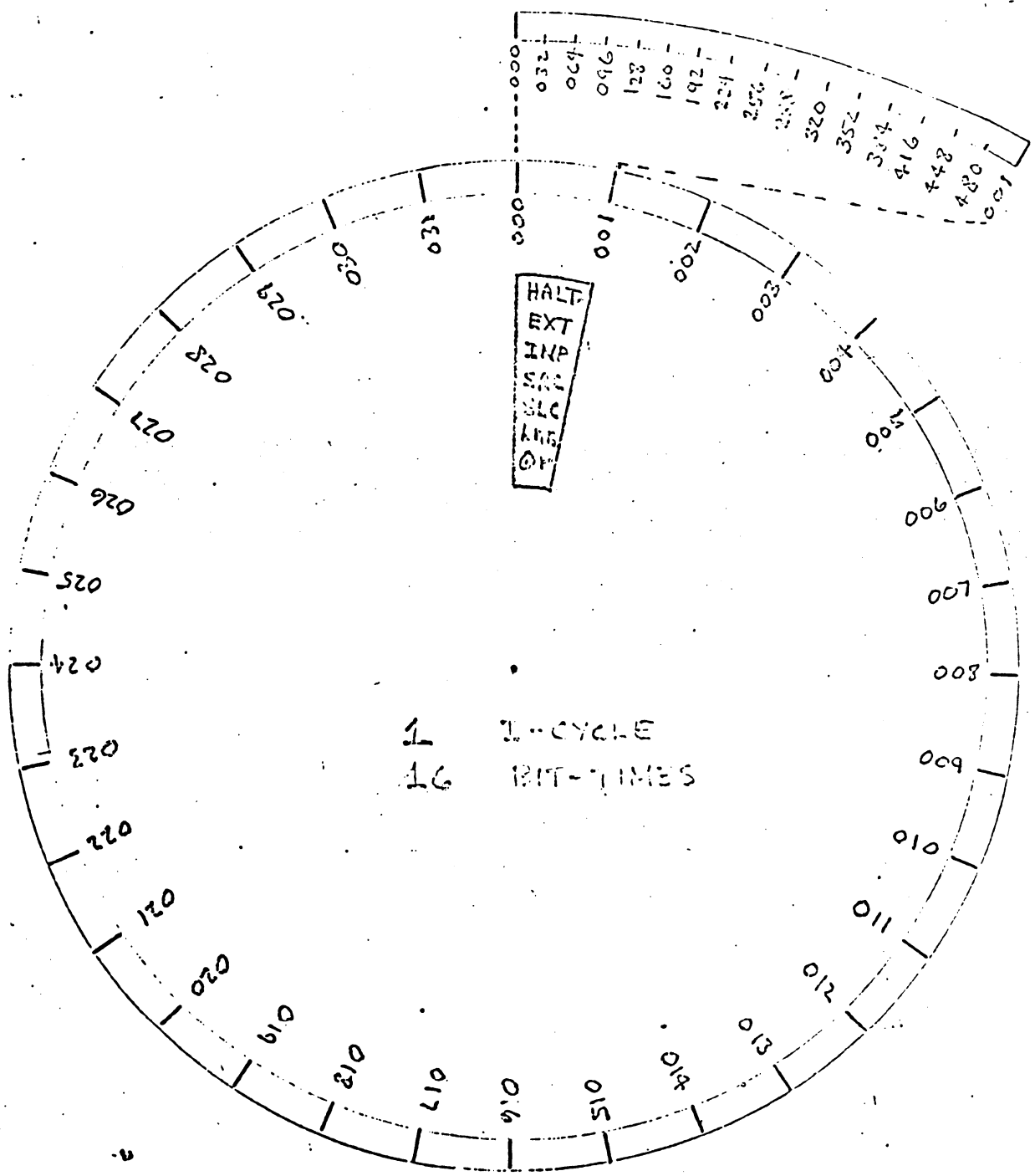


CTC DP2200
INSTRUCTION CYCLE TIMING

5/12/70 RWB

REGISTER INSTRUCTION CYCLE-TIMES

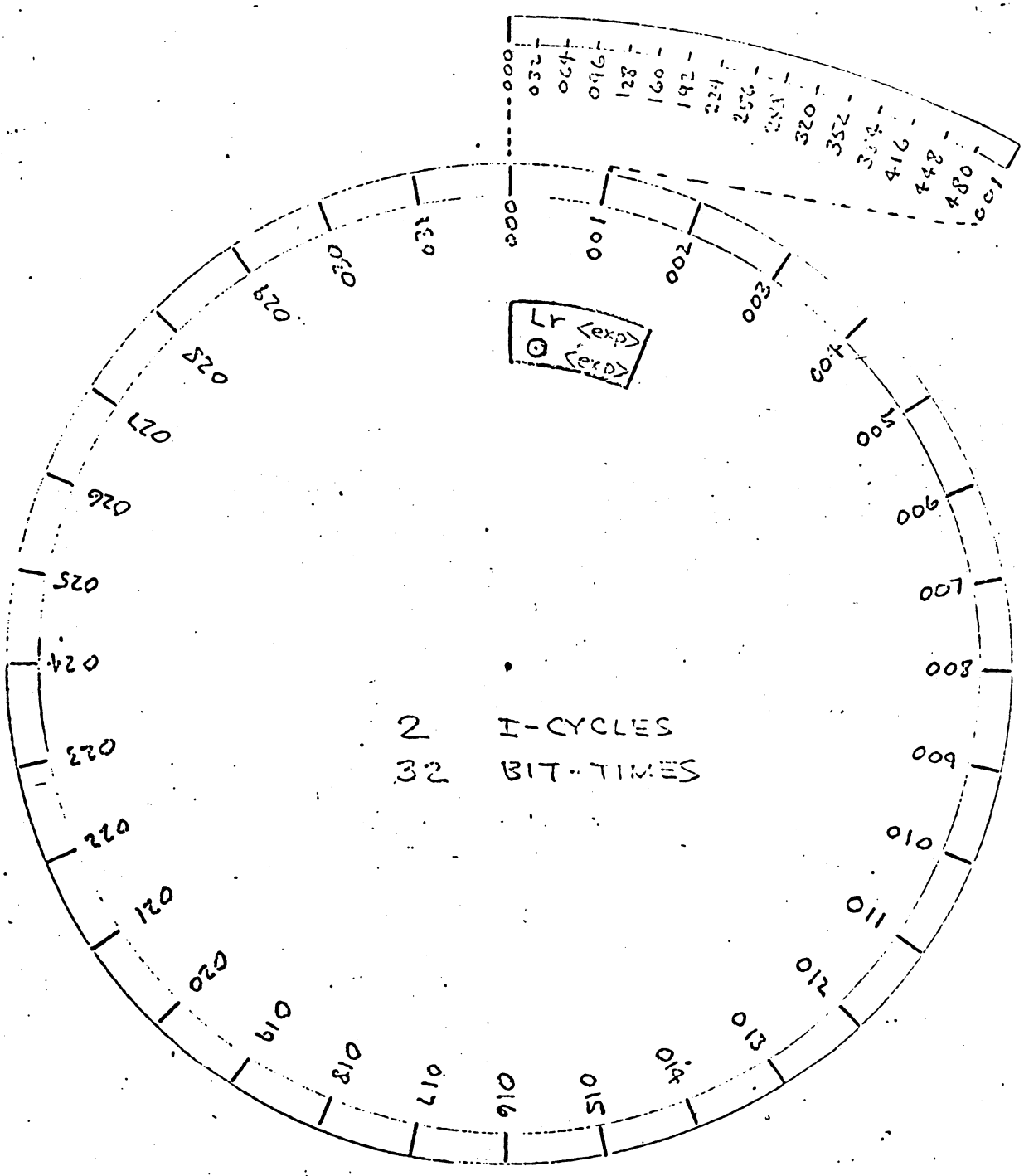
GMR 5/12/70



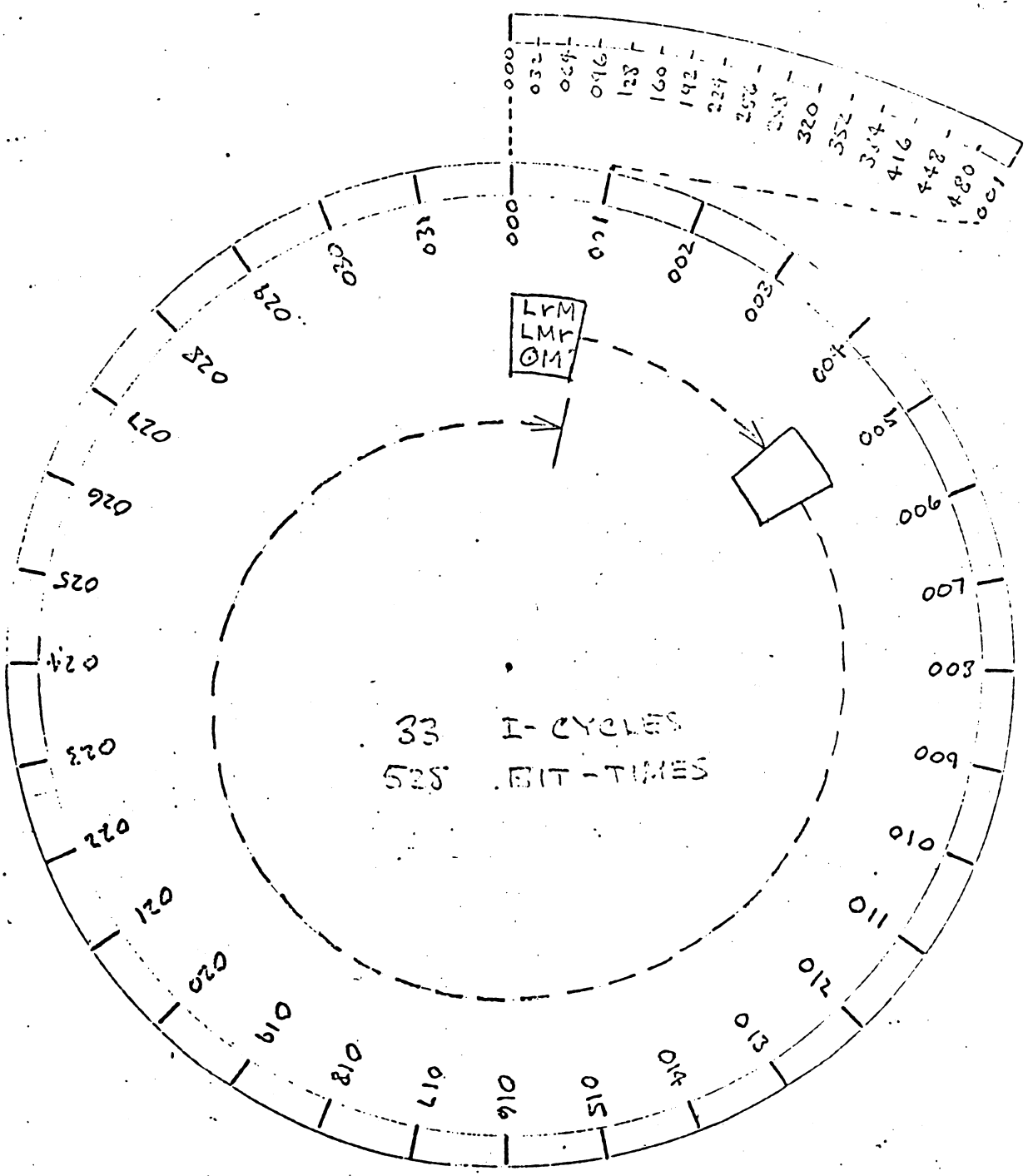
IMMEDIATE ENVIRONMENT

CYCLE - TIMES

GMB 5/12/70

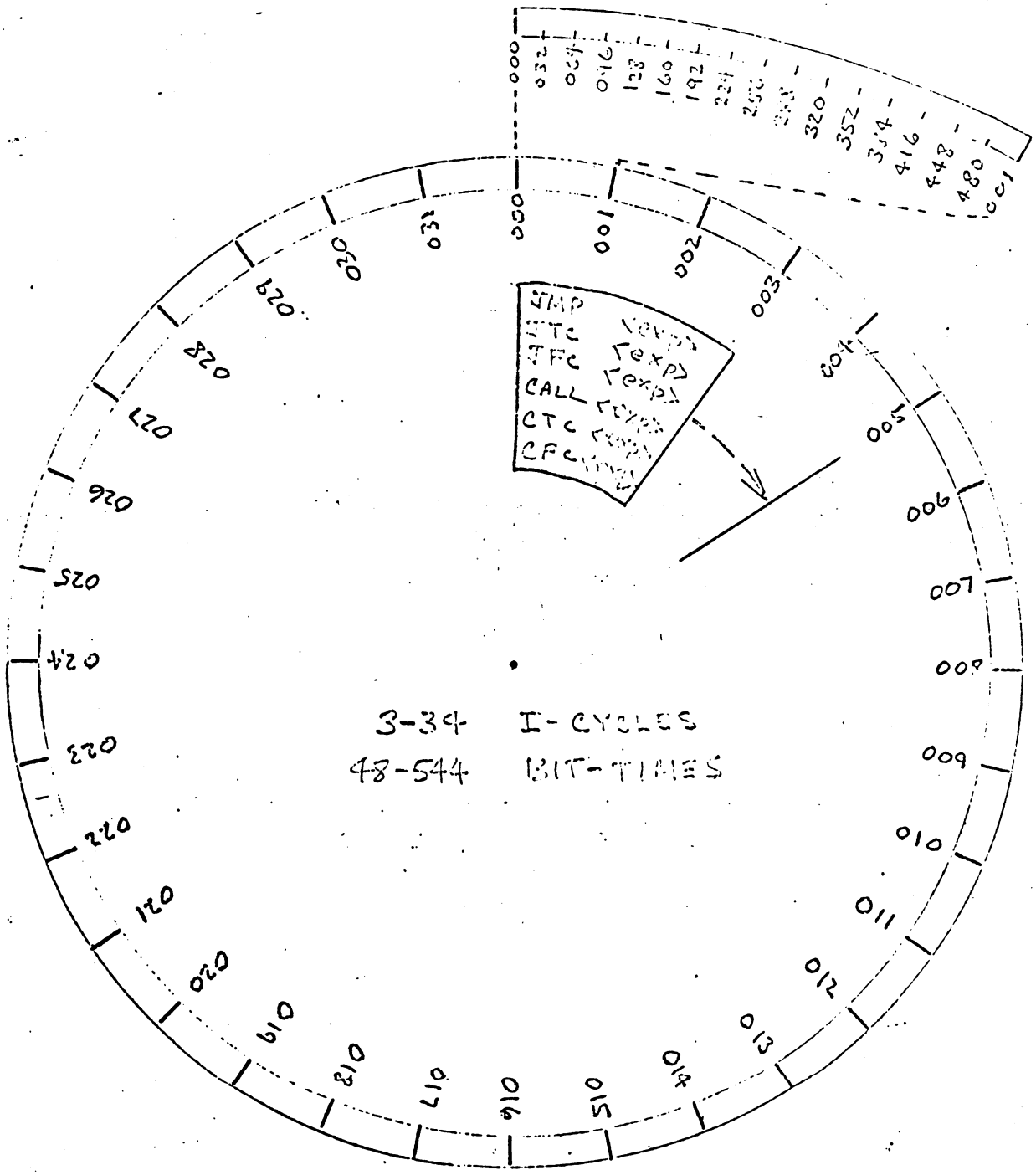


MEMORY INSTRUCTION CYCLE-TIMES

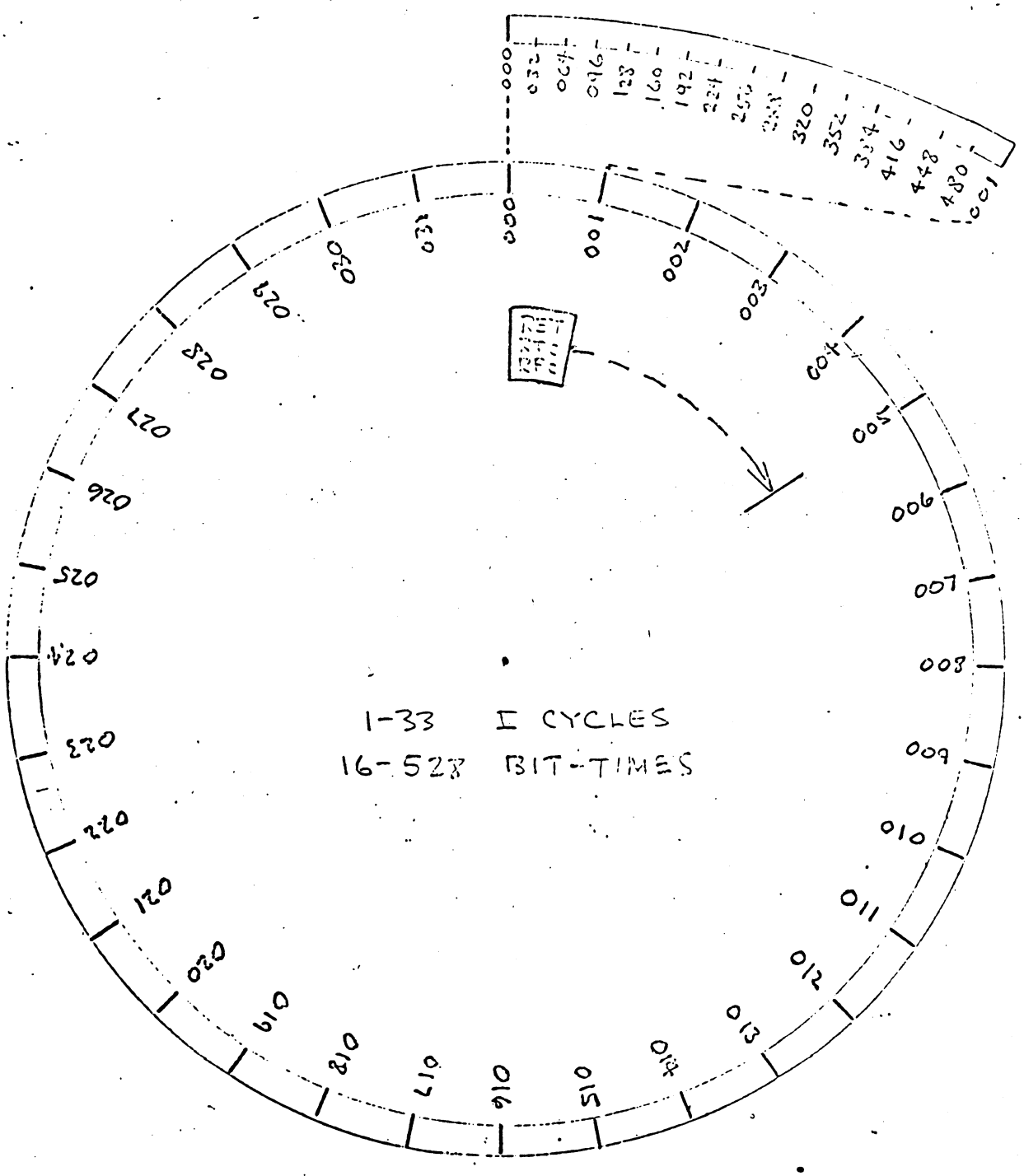


JUMP INSTRUCTION
CYCLE-TIMES

SMB 5/12/70



RETURN INSTRUCTION
CYCLE-TIMES
Sine Sigma



CTC DP2200
INSTRUCTION SET
5/12/70 LWK

MNEMONIC	OPERATION	$\phi I_7 I_6$	$I_5 I_4 I_3$	$I_2 I_1 I_0$
Lr1r2	(r1) ← (r2)	3	d	s
LrM	(r) ← MEM			
LMr	MEM ← (r)			
Lr,<exp>	(r) ← <exp>	0	d	6
⊙r	A ← A ⊙ (r), CY/SP ← ⊙/A	2	p	s
⊙M	A ← A ⊙ MEM, CY/SP ← ⊙/A			
⊙,<exp>	A ← A ⊙ <exp>, CY/SP ← ⊙/A	0	p	4
JMP,<exp>	P ← <exp>	1	TRUE/ff	CONDITION
JTC,<exp>	c ⊃ P ← <exp> ; c̄ ⊃ P ← P+3			
JFC,<exp>	c̄ ⊃ P ← <exp> ; c ⊃ P ← P+3			
CALL,<exp>	STACK ← P, JMP			
CTC,<exp>	c ⊃ STACK ← P, JTC			
CFC,<exp>	c̄ ⊃ STACK ← P, JFC			
RETURN	P ← STACK	0	TRUE/ff	CONDITION×0
RTC	c ⊃ P ← STACK			
RFC	c̄ ⊃ P ← STACK			
SLC	A ← 1↓A, CARRY ← A_7	0	00	2
SRC	A ← 1↑A, CARRY ← A_0			
INPUT	A ← IDL	1	00x	xx1
EXT	EX ← 1	1	xxx	xx1
HALT	STOP ← 0	0	0	00x
		3	7	7

⊙	p
AD	0
AC	1
SU	2
SB	3
ND	4
XR	5
OR	6
CP	7

r	s,d
A	0
B	1
C	2
D	3
E	4
H	5
L	6
M	7

c	ff
CARRY	00
ZERO	01
SIGN	10
PARITY	11

INTERRUPTS

*HALT ⊃ STOP ← 0
*CONT ⊃ STOP ← 0
*RST ⊃ ENTRY ⊃ P ← 101

INSTRUCTION	ENTRY ⇒ ITO DATA FLOW < LMB 4/10/70		PG 1/4 >
RESTART	$REST	0	STOP ← '1'
		1	
		4	RWI ← '101'
		S,E	P ← 0
		F	STOP ← '0'
		•	
		•	
		•	
LBA	P=T	^	STOP ← '1', M ⇐ MEM
		1	I ⇐ M
		4	RWI ← '101'
		S,E	B ← A, A ← A, P ← P+1
		F	STOP ← '0'
LCM	P=T	0	STOP ← '1' M ⇐ MEM
		1	I ⇐ M
		4	RWI ← '100', STACK ⇐ P
		S,E	P ← H@L, H ← H, L ← L
		F	STOP ← '0'
		•	
		•	
		•	
	P=T	0	STOP ← '1', M ⇐ MEM
		1	
		4	P ⇐ STACK, RWI ← '101'
		S,E	C ← M, P ← P+1
		F	STOP ← '0'
		•	
		•	
		•	
LD <exp>	P=T	0	STOP ← '1', M ⇐ MEM
		1	I ⇐ M
		4	RWI ← '100'
		S,E	P ← P+1
		F	STOP ← '0'
	P=T	0	STOP ← '1', M ⇐ MEM
		1	
	"	4	RWI ← '101'
		S,E	D ← M
		F	STOP ← '0'

INSTRUCTION	ENTRY POINT	DATA FLOW < GWB 4/19/76	PG 2/47
LME	P=T	0	STOP ← '1', M ⇐ MEM
		1	I ← M
		4	RWI ← '000', STACK ⇐ P
		S,E	P ← H ⊙ L, H ← H, L ← L, M ← E
		F	STOP ← '0'
			.
			.
			.
	P=T	0	STOP ← '1' ~~M ⇐ MEM~~ MEM ⇐ M
		1	
		4	RWI ← '101', P ⇐ STACK
		S,E	P ← P+1
		F	STOP ← '0'
			.
			.
			.
⊙H	P=T	0	STOP ← '1', M ⇐ MEM
		1	I ⇐ M
		4	RWI ← '101'
		S,E	A ← A ⊙ H ⊙ CARRY, P ← P+1
		F	STOP ← '0'
⊙M	P=T	0	STOP ← '1', M ⇐ MEM
		1	I ⇐ M
		4	RWI ← '100' STACK ⇐ P
		S,E	P ← H ⊕ L
		F	STOP ← '0'
			.
			.
			.
	P=T	0	STOP ← '1', M ⇐ MEM
		1	~~I ⇐ M~~
		4	RWI ← '101', P ⇐ STACK
		S,E	P ← P+1, A ← A ⊙ M ⊙ CARRY
		F	STOP ← '0'
			.
	"		.
			.

INSTRUCTION	ENTRY ⊃ IT ⊃ DATA FLOW <SJWB 4/10/76 PG 3/4 >		
⊙ <exp>	P=T	0	STOP ← '1', M ⇐ MEM
		1	I ⇐ M
		4	RWI ← '100'
		S,E	P ← P+1
		F	STOP ← '0'
	P=T	0	STOP ← '1', M ⇐ MEM
		1	
		4	RWI ← '101'
		S,E	A ← A ⊙ M ⊙ CARRY, P ← P+1
		F	STOP ← '0'
JMP <exp>	P=T	0	STOP ← '1', M ⇐ MEM
CALL <exp>		1	I ⇐ M
		4	RWI ← '100'
		S,E	P ← P+1
		F	STOP ← '0'
	P=T	0	STOP ← '1', M ⇐ MEM
		1	
		4	RWI ← '100'
		S,E	P ← P+1, N ← M
		F	STOP ← '0'
	P=T	0	STOP ← '1' M ⇐ MEM
		1	
		4	RWI ← '101', PUSH ⊃ STACK ⇐ P
		S,E	P ← N ⊕ M
		F	STOP ← '0'
		•	
		•	
		•	
JFc <exp>	P=T	0	STOP ← '1', M ⇐ MEM
CFc <exp>		1	I ⇐ M
		4	RWI ← '100'
		S,E	P ← P+1
		F	STOP ← '0'
	P=T	0	STOP ← '1' M ⇐ MEM
		1	
		4	RWI ← '100'
		S,E	P ← P+1, N ← M
		F	STOP ← '0'
	P=T	0	STOP ← '1', M ⇐ MEM
		1	
	"	4	RWI ← '101', PUSH ⊃ STACK ⇐ P
		S,E	(c) ⊃ P ← N ⊕ M, (c) ⊃ P ← P+1
		F	STOP ← '0'

[REVERSE CONDITIONS FOR JTc & CTc

INSTRUCTION	ENTRY ⊃ IT ⊃ DATA FLOW <QWB 4/15/70 PG 4/4>		
RETURN	P=T	0	STOP ← '1', M ⇐ MEM
		1	I ⇐ M
		4	P ← STACK, RWI ← '101'
		S,E	P ⇐ P+1
		F	STOP ← '0'
		.	
		.	
		.	
RFC	P=T	0	STOP ← '1', M ⇐ MEM
RTC		1	I ⇐ M
		4	RWI ← '101', T/(C)∨F/(C) ⊃ P ⇐ STACK
		S,E	P ← P+1
		F	STOP ← '0'
		.	
		.	
		.	
SLC	P=T	0	STOP ← '1', M ⇐ MEM
SRC		1	I ⇐ M
		4	RWI ← '101',
		S,E	LEFT ⊃ A ← 1↓A, RIGHT ⊃ A ← 1↑A, P ← P+1
		F	STOP ← '0'
INPUT	P=T	0	STOP ← '1', M ⇐ MEM
		1	I ⇐ M
		4	RWI ← '101', A ⇐ IOL
		S,E	P ← P+1
		F	STOP ← '0'
EXT	P=T	0	STOP ← '1', M ⇐ MEM
		1	I ⇐ M
		4	RWI ← '10', STA ← I/O
		S,E	P ← P+1
		F	STOP ← '0'
HALT	P=T	0	STOP ← 1, M ⇐ MEM
		1	I ⇐ M
		4	RWI ← '101'
		S,E	P ← P+1
		F	STOP ← '0'
			#HALT interlocks STOP at first IT=F
	"		#CONT ⊃ STOP ← '0'

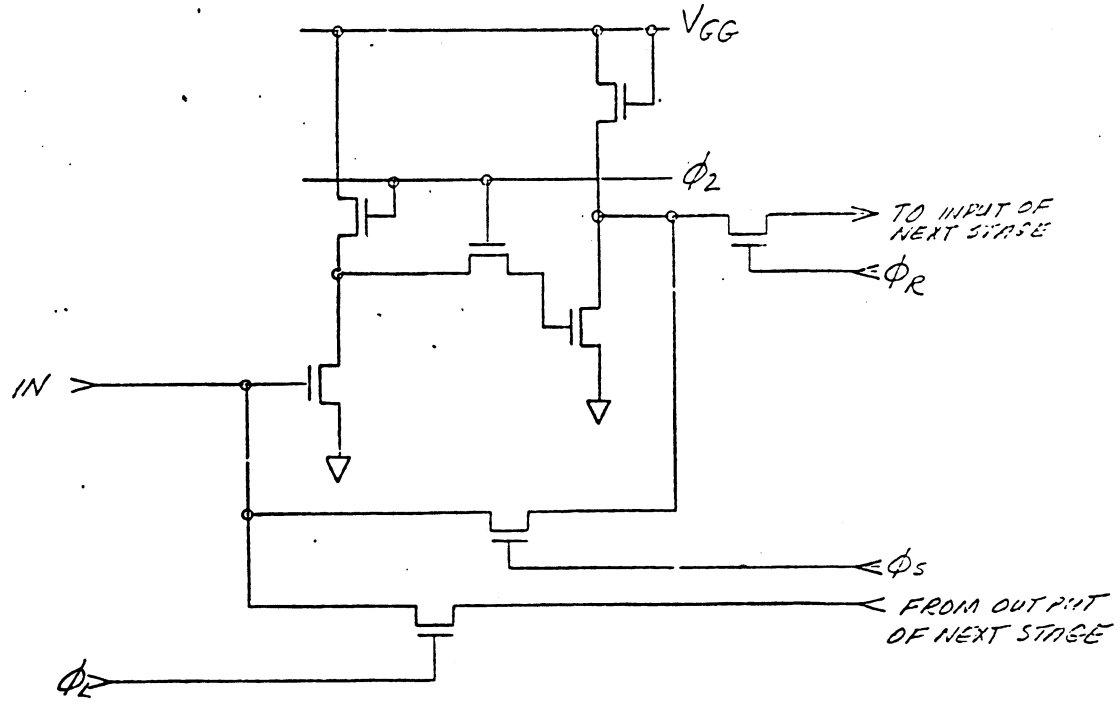
CTC-DP2200

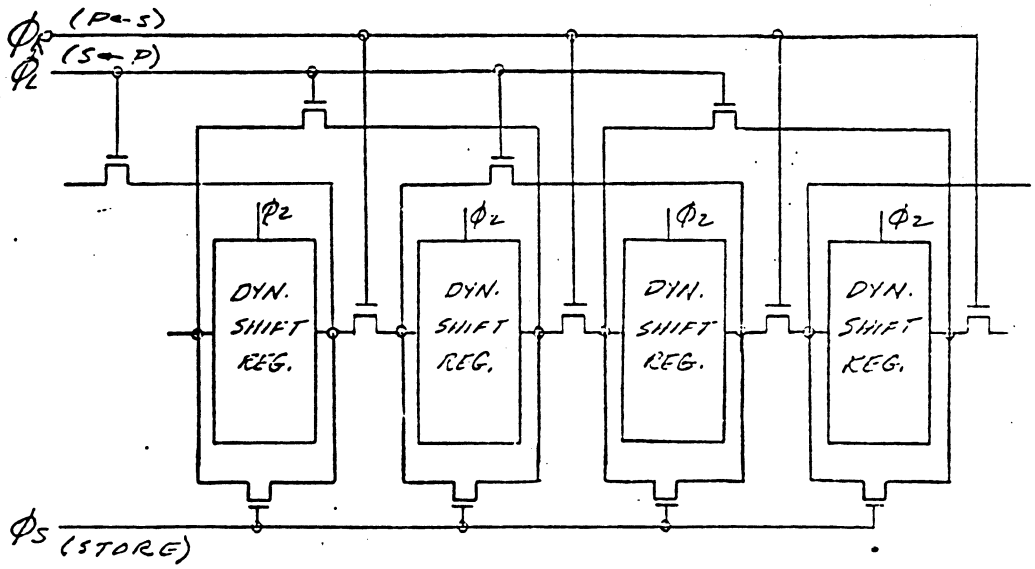
P-Stack Chip

Block Diagram

JVD/ERC

5/13/70



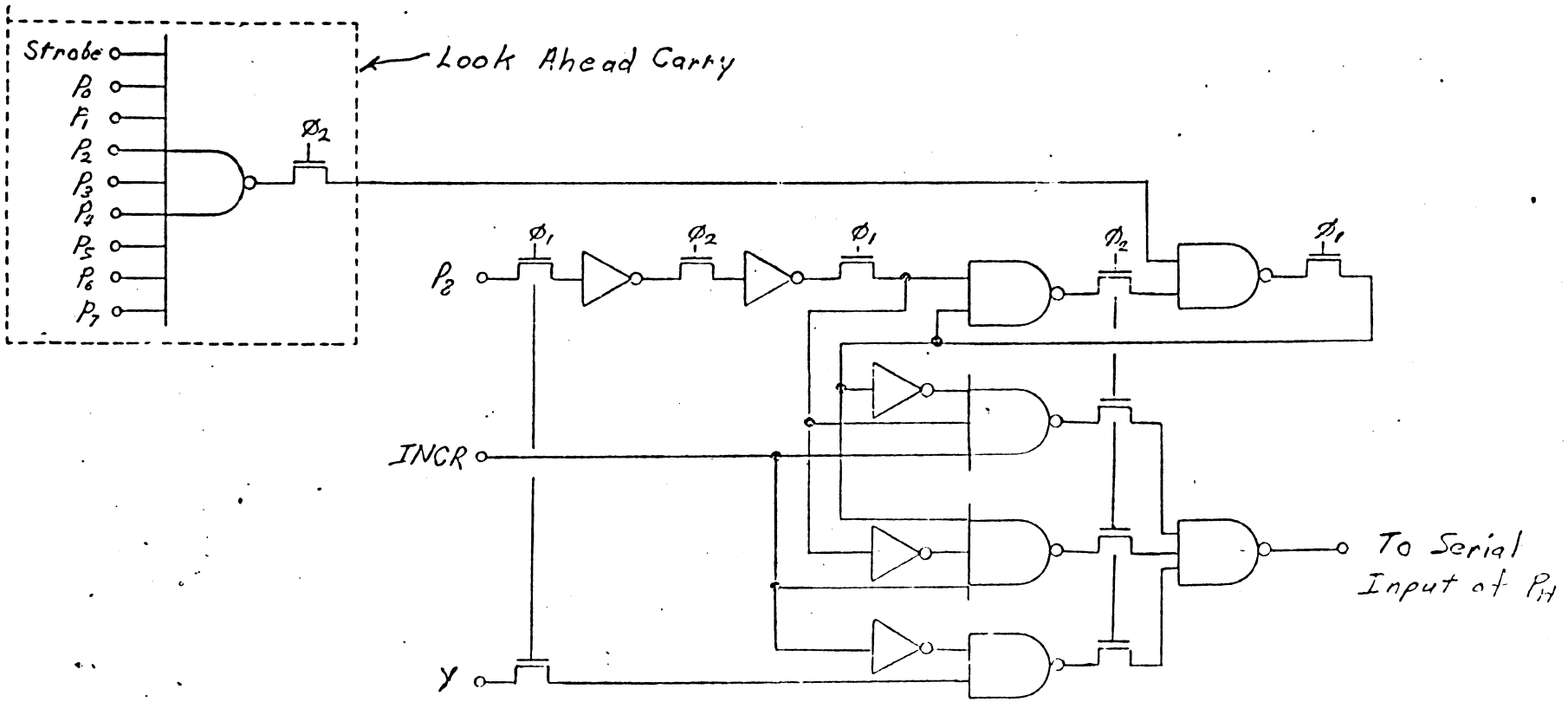


DP 2200 P-STACK BI-DIRECTIONAL SHIFT REGISTER

1/8/70

CTC-DP2200

P-Register and Push-down Stack
Add 1 and Gating Logic for P_H



PROPRIETARY INFORMATION

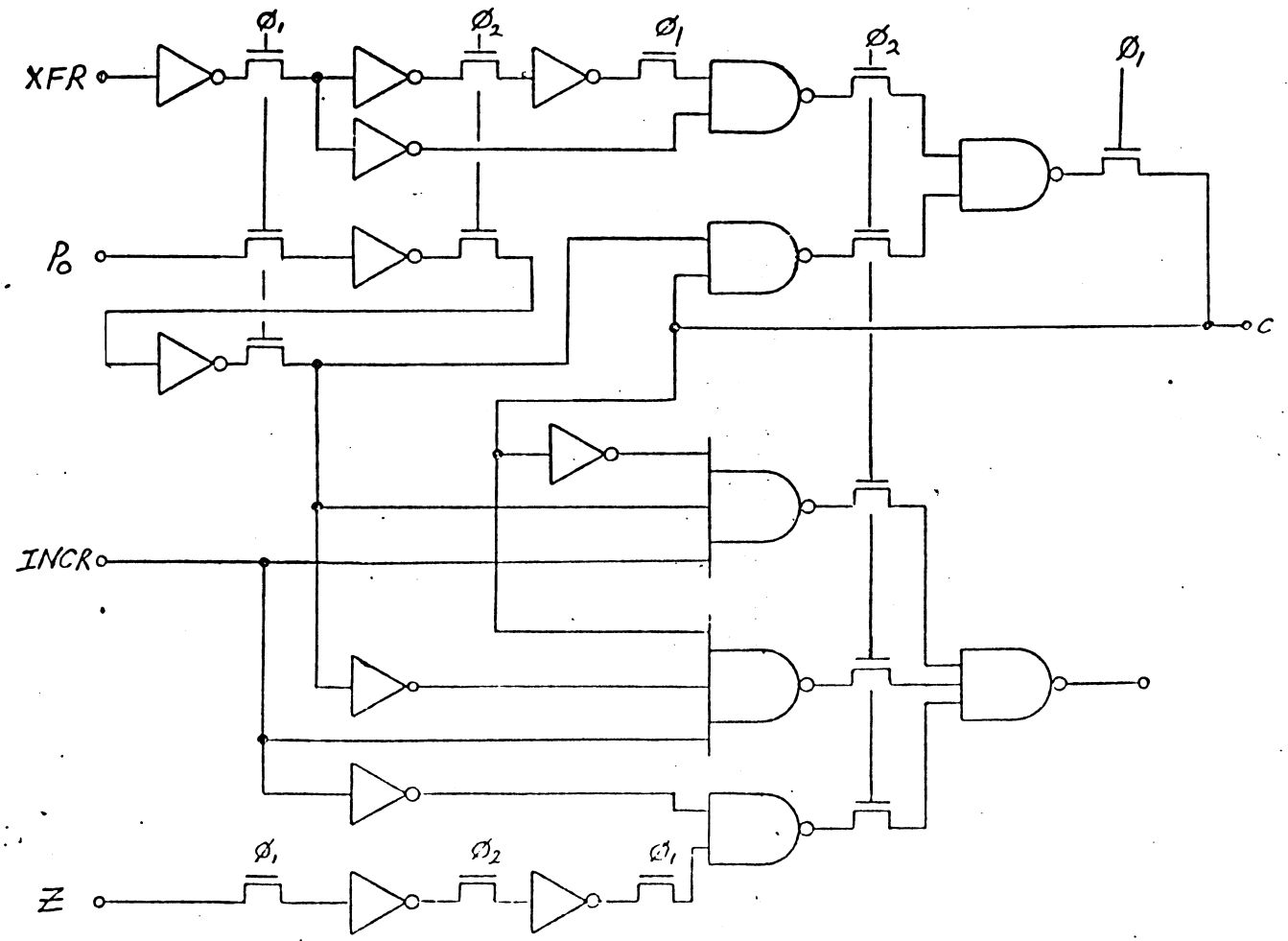
SHEET

E.R.C.
5/13/74

CTC DP2200

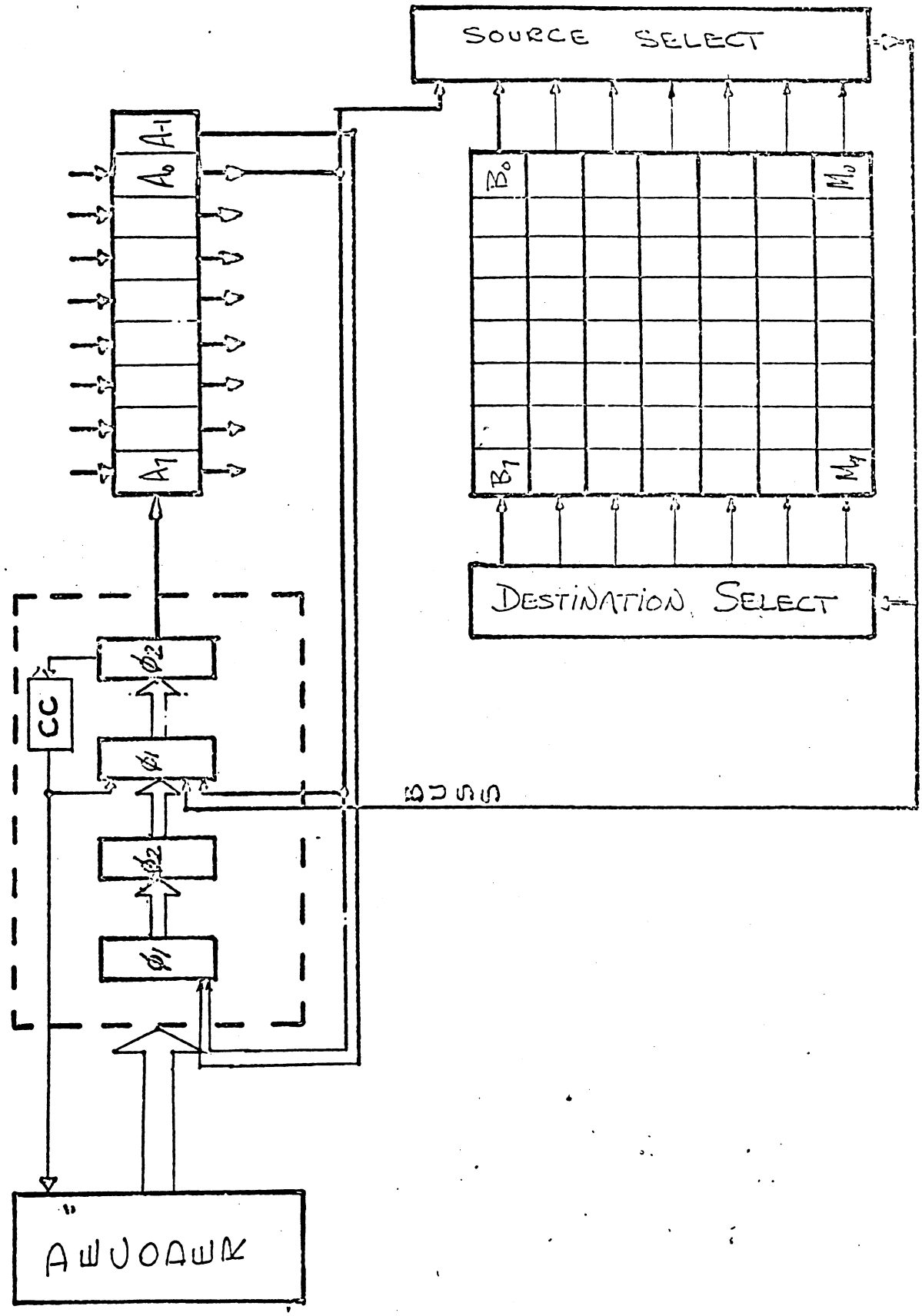
P-Register and Push-down Stack

Add 1 and gating logic for P_L



ERC
5/13/70

ALU - Register Block Diagram



CTC DP 2200
REGISTER EQUATIONS
5/12/70 AWB

$$D(\text{CARRY}) = A_{-2} \quad (\text{SHIFT})$$
$$+ CB \quad (\bar{I}_5 + I_4 I_3) \quad (\text{ARILOG})$$
$$+ \text{CARRY} \quad (\overline{\text{ARILOG}})$$

$$D(\text{ZERO}) = \text{ITG} \quad (\text{ARILOG})$$
$$+ \text{ZERO} \quad (\text{ARILOG}) \left[D(A_7) \cdot \overline{I_5 I_4 I_3} + \right.$$
$$\left. + (\bar{A}_{-1} Y CB + A_{-1} \bar{Y} CB + A_{-1} Y \bar{CB} + \bar{A}_{-1} \bar{Y} \bar{CB}) \cdot I_5 I_4 I_3 \right]$$
$$+ \text{ZERO} \quad (\overline{\text{ARILOG}})$$

$$D(\text{SIGN}) = (\text{ARILOG}) \left[D(A_7) \cdot \overline{I_5 I_4 I_3} + \right.$$
$$\left. + (A_{-1} \bar{Y} CB + \bar{A}_{-1} Y \bar{CB} + \bar{A}_{-1} \bar{Y} CB + A_{-1} Y CB) I_5 I_4 I_3 \right]$$
$$+ \text{SIGN} \cdot \overline{\text{ARILOG}}$$

$$D(\text{PARITY}) = \overline{\text{ITG}} \cdot \text{ARILOG} \left[(D(A_7) \cdot \overline{\text{PARITY}} + \overline{D(A_7)} \cdot \text{PARITY}) \overline{I_5 I_4 I_3} \right.$$
$$+ (\bar{A}_{-1} Y CB + A_{-1} \bar{Y} CB + A_{-1} Y \bar{CB} + \bar{A}_{-1} \bar{Y} \bar{CB}] \text{ PARITY}$$
$$\left. + [A_{-1} \bar{Y} \bar{CB} + \bar{A}_{-1} Y \bar{CB} + \bar{A}_{-1} \bar{Y} CB + A_{-1} Y CB] \overline{\text{PARITY}} \right) \cdot I_5 I_4 I_3$$
$$+ \text{PARITY} \quad (\overline{\text{ARILOG}})$$

$$D(B_7) = (\text{DEN } \bar{I}_5 \bar{I}_4 I_3) \cdot Y + (\overline{\text{-DITTO-}}) \cdot B_{-1}$$
$$D(C_7) = (\text{DEN } \bar{I}_5 I_4 \bar{I}_3) \cdot Y + (\overline{\text{-DITTO-}}) \cdot C_{-1}$$
$$D(D_7) = (\text{DEN } \bar{I}_5 I_4 I_3) \cdot Y + (\overline{\text{-DITTO-}}) \cdot D_{-1}$$
$$D(E_7) = (\text{DEN } I_5 \bar{I}_4 \bar{I}_3) \cdot Y + (\overline{\text{-DITTO-}}) \cdot E_{-1}$$
$$D(H_7) = (\text{DEN } I_5 \bar{I}_4 I_3) \cdot Y + (\overline{\text{-DITTO-}}) \cdot H_{-1}$$
$$D(L_7) = (\text{DEN } I_5 I_4 \bar{I}_3) \cdot Y + (\overline{\text{-DITTO-}}) \cdot L_{-1}$$
$$D(M_7) = (\text{DEN } I_5 I_4 I_3) \cdot Y + (\overline{\text{-DITTO-}}) \cdot M_{-1}$$
$$D(N_7) = M_{-1}$$

NOTE! 1-BIT INTRINSIC DELAY
ASSUMED FOR ALL EQUATIONS

CTC D???? ALU EQUATIONS 5/12/70 [illegible]

$D(A7) = A_{-1}\bar{Y}\,\overline{CB}\,(\bar{I}_5 + \bar{I}_4 I_3)(ARILOG)$

$+ \bar{A}_{-1} Y \overline{CB}$ (") (")

$+ \bar{A}_{-1}\bar{Y}\,CB\,(\bar{I}_5)$ (")

$+ A_{-1} Y\,CB\,(\bar{I}_5)$ (")

$+ A_{-1}\cdot Y\,(I_5 \bar{I}_4 \bar{I}_3)$ (")

$+ (A_{-1} + Y)(I_5 I_4 \bar{I}_3)$ (")

$+ A_0\,(SLC)$

$+ (A_{-1}\cdot\overline{ITG} + A_6\cdot ITG)(SLC)$

$+ Y\,(\bar{I}_5 \bar{I}_4 \bar{I}_3\,DEN)$

$+ A_{-1}\,(I_5 I_4 I_3\cdot ARILOG + \bar{I}_2 \bar{I}_1 \bar{I}_0\cdot SEN + KEEPA)$

$CB = CARRY\cdot(ITS)(\bar{I}_5\cdot I_3)$

$+ A_{-1} Y\,CB\,(\overline{ITS})(\bar{I}_5 \bar{I}_4)$

$+ A_{-1} Y\,CB$ (") (")

$+ A_{-1} Y\,CB$ (") $(\bar{I}_5 + I_4 I_3)$

$+ A_{-1} Y\,CB$ (") (")

$+ A_{-1} Y\,CB$ (") $(\bar{I}_5\cdot I_4 + I_4 I_3)$

$+ A_{-1} Y\,CB$ (") (")

$Y = (SEN)(\bar{I}_2 \bar{I}_1 \bar{I}_0) A_0$

$+$ (") $(\bar{I}_2 \bar{I}_1 I_0) B_0$

$+$ (") $(\bar{I}_2 I_1 \bar{I}_0) C_0$

$+$ (") $(\bar{I}_2 I_1 I_0) D_0$

$+$ (") $(I_2 \bar{I}_1 \bar{I}_0) E_0$

$+$ (") $(I_2 \bar{I}_1 I_0) H_0$

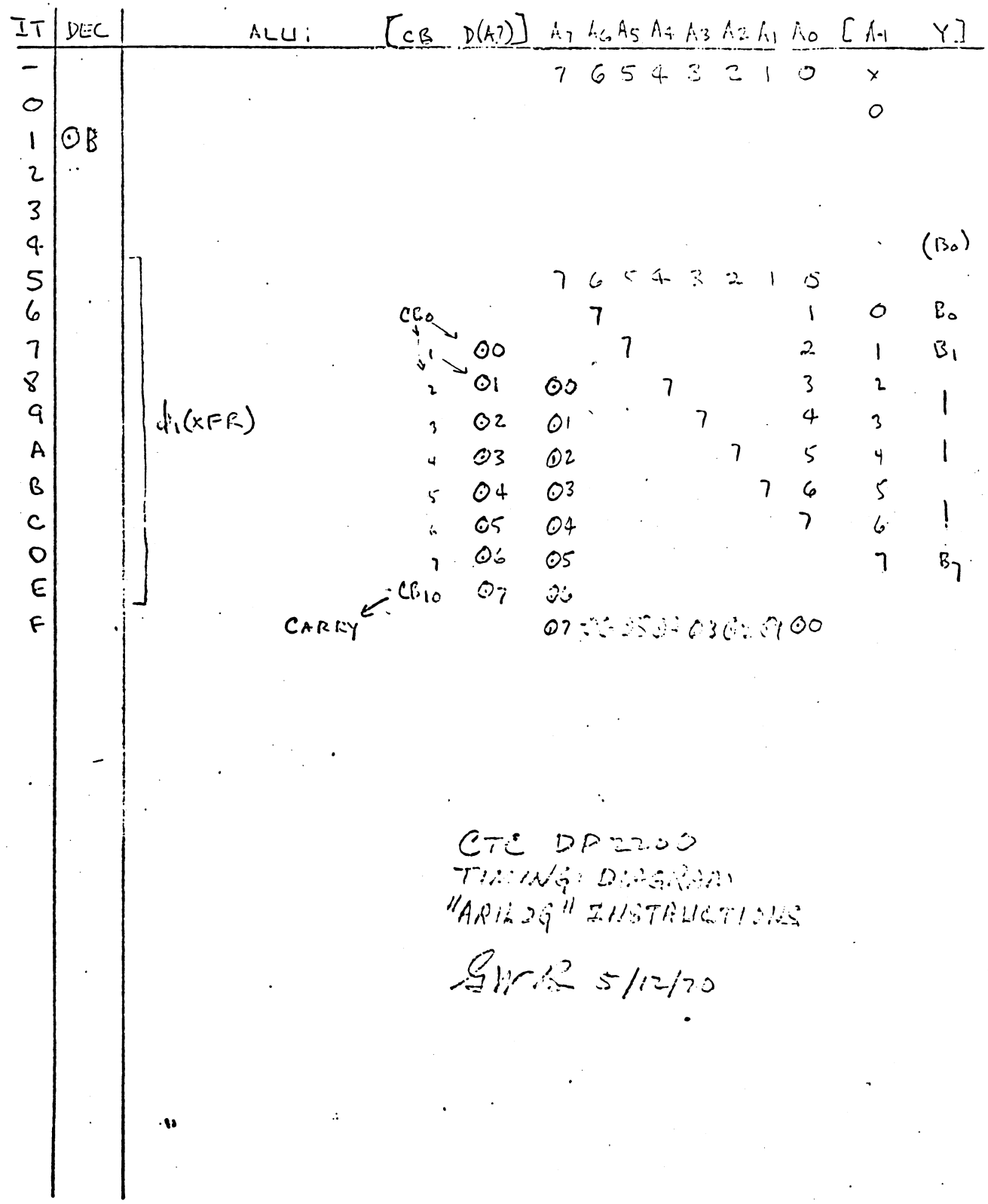
$+$ (") $(I_2 I_1 \bar{I}_0) L_0$

$+$ [(") $(I_2 I_1 I_0)$ + MMM] M_0

$Z = NNN\cdot M_0 + \overline{NNN}\cdot L_0$

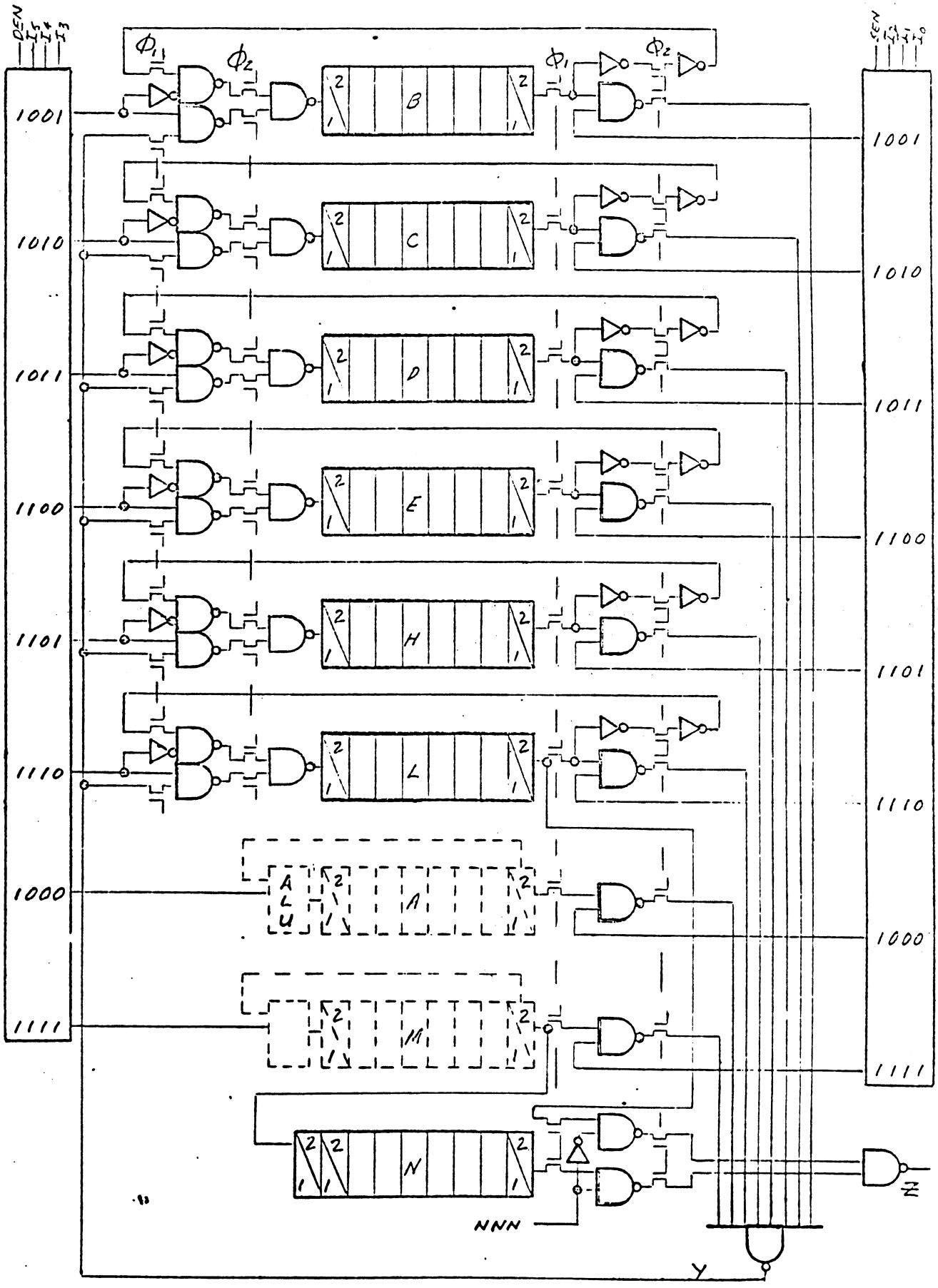
NOTE

1-BIT INTRINSIC DELAY ASSUMED FOR ALL EQUATIONS



CTC DP2200
TIMING DIAGRAM
"ARILOG" INSTRUCTIONS

GWK 5/12/70

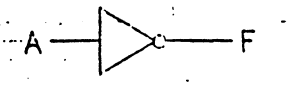


CTC DP2200 REGISTER LOGIC

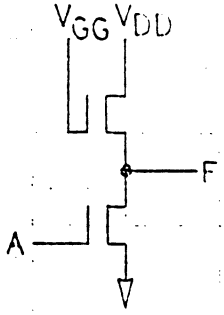
JD.

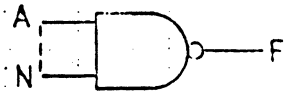
CTC DP 2200

LOGIC SYMBOL DESCRIPTION

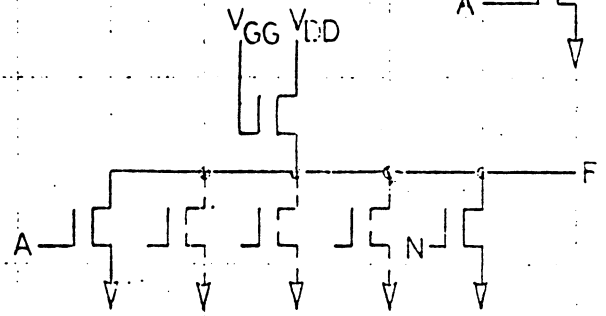


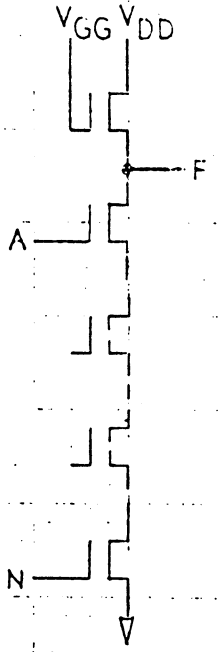
INVERTER



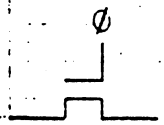


NAND



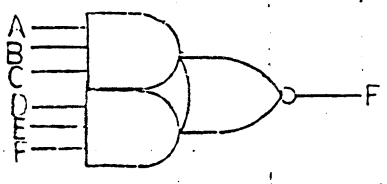


NOR

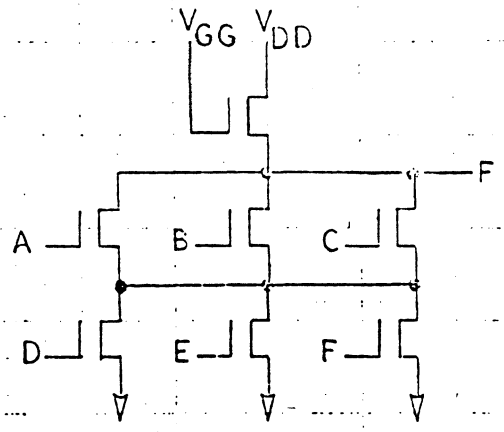


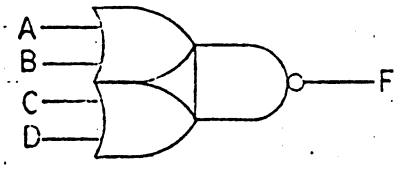
TRANSFER GATE

COMPLEX GATES

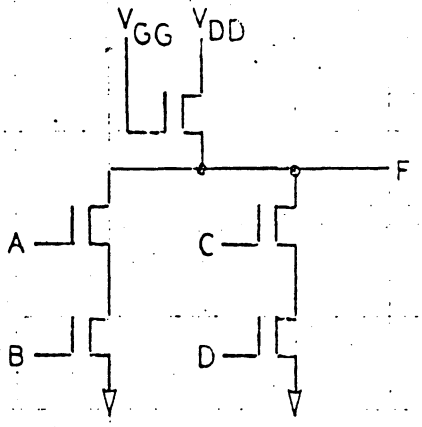


$\overline{ABC+DEF}$

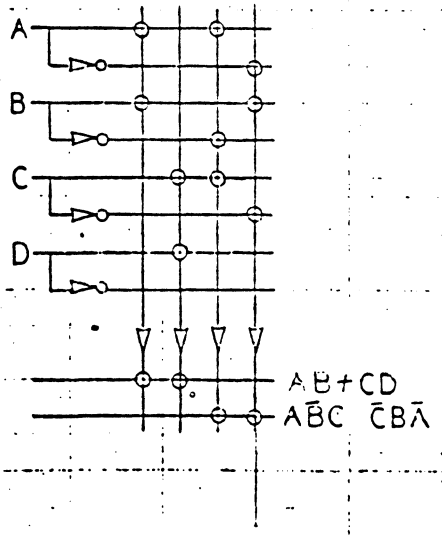


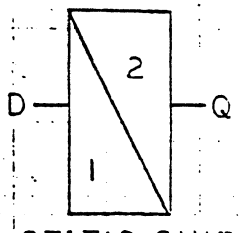


$\overline{(A+B)(C+D)}$

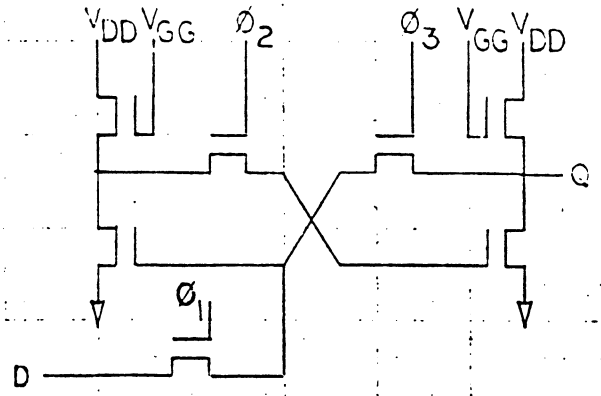


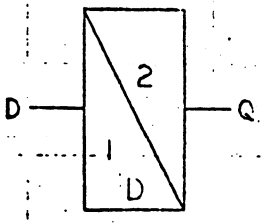
DECODE MATRIX



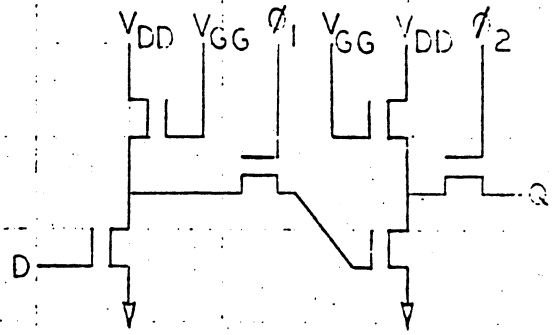


STATIC SHIFT REGISTER

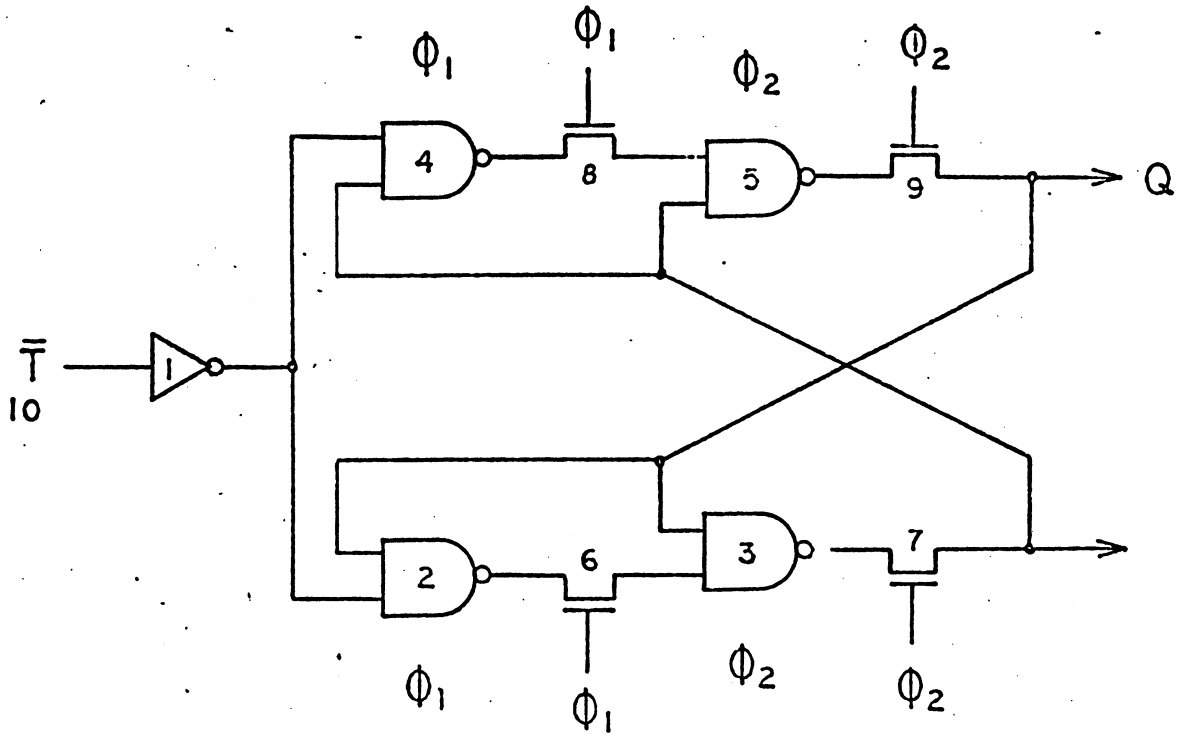




DYNAMIC SHIFT REGISTER



NOTE: IN SOME CASES V_{GG} MAY BE REPACED BY AN AN APPROPRIATE CLOCK



TOGGLE FLIP FLOP

PROPRIETARY INFORMATION

SIZE		SHEET
SYM	REVISION	

MATERIAL		
FINISH	NEXT ASSEMBLY	QTY
	TOLERANCES UNLESS SPECIFIED	
DRAFTSMAN DATE	XXXX ± 0005 XXX ± 005 XX ± 010 X ± 030 ANGLES ± 15 MIN (± 0.4 10 INCHES) AXIS OF TAPPED HOLES 90° ±1° MACHINED DIAMETERS CONCENTRICITY .004 T.I.R. ALL DIMENSIONS ARE IN INCHES REMOVE ALL BURRS AND SHARP EDGES DO NOT SCALE THIS DRAWING	
DESIGNER DATE		
CHECKER DATE		
ENGINEER DATE		
APPROVED DATE	HOLE TOLERANCES 0.35 THRU .125 + .004 − .001 126 THRU 250 + .005 − .002 251 THRU 500 + .006 − .002 501 THRU 750 + .008 − .002 751 THRU 1.000 + .010 − .003 1.001 THRU 2.000 + .012 − .001	SURFACE ROUGHNESS
RELEASED DATE		

TEXAS INSTRUMENTS INCORPORATED
SEMICONDUCTOR COMPONENTS DIVISION

CODE IDENT NO 01295

TITLE

EXAMPLE OF LOGIC SIMULATION IN SIMOS

CTC DP 2200

SCALE		SHEET

80 COLUMN DATA FORM TI-1378-A

SIMOS CODING FORMAT

DATE | PAGE | OF | SHEET

☐ KEYPUNCH, VERIFY, LIST, AND RETURN TO REQUESTER AT:

☐ 7074 ☐ 1620 ☐ 1401 ☐

EXTENSION NO.

☐ KEYPUNCH, VERIFY, LIST, AND ADD TO REQUESTER'S DECK NO.

RUN AND RETURN TO REQUESTER AT:

REQUESTOR	PROGRAM NO.	DIVISION	COST CENTER	E.O./O.O./W.O./ACCOUNT NO.

A SIZE

```
      1    5    10   15   20   25   30   35   40   45   50   55   60   65   70   75   80
01    1 TIG  1    10                                                    21
02    2 T2G  1     1   9
03    3 T2G  2     6   9
04    4 T2G  1     1   7
05    5 T2G  2     7   8
06    6 CKG  1     2                                                    3
07    7 CKG  2     3                                                    4
08    8 CKG  1     4                                                    5
09    9 CKG  2     5                                                    6
10    10 GEN       503  12   4    8                                     0          1
11
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LOGICAL SIMULATION OF THE CTC DP2200 ARITHMETIC / LOGIC UNIT

		3 66 55	4 3 9	4 3 8	4 3 7	4 3 6	4 3 5	4 3 4	4 3 3	4 3 2	4 3 1	4 3 0	33333333 33334444 67890123	4 5 0	3 4 4	3 3 5	3 1 1	3 1 3	3 2 5	3 3 3	3 3 4	3 2 1	3 1 4	3 1 5	3 1 6
1	1	00	0	0	0	0	0	0	0	0	0	0	00000000	0	0	0	1	1	0	0	0	1	1	1	0
2	0	00	0	0	0	0	0	0	0	0	0	0	00000000	0	0	1	1	1	0	0	1	1	1	1	0
3	1	00	0	0	0	0	0	0	0	0	0	0	00000000	0	0	1	1	1	0	0	1	1	1	1	0
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32	0	01	1	1	0	1	1	1	1	1	1	0	11111110	1	0	1	1	0	1	0	1	0	1	1	0
33	1	11	1	1	0	1	1	1	1	1	1	0	11111110	1	0	1	1	0	1	0	1	0	1	1	0
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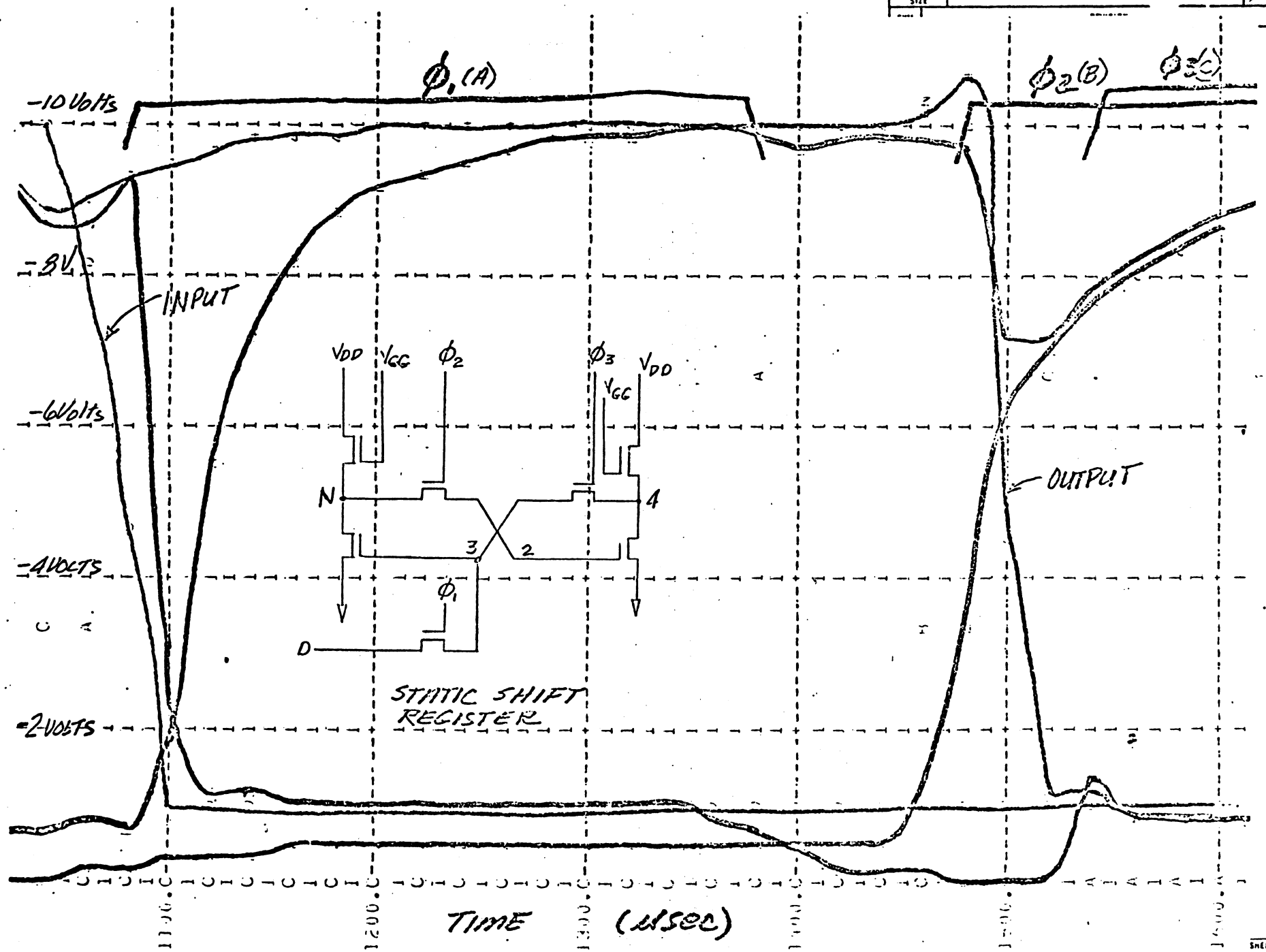
PROPRIETARY INFORMATION



MOSMOD EXAMPLE