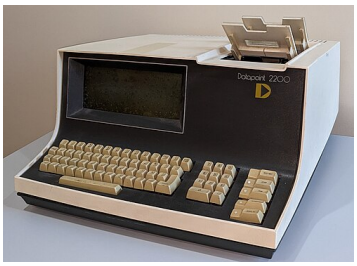
Datapoint 2200

The **Datapoint 2200** was a mass-produced programmable terminal usable as a computer, designed by Computer Terminal Corporation (CTC) founders Phil Ray and Gus Roche[2] and announced by CTC in June 1970 (with units shipping in 1971). It was initially presented by CTC as a versatile and cost-efficient terminal for connecting to a wide variety of mainframes by loading various terminal emulations from tape rather than being hardwired as most contemporary terminals, including their earlier Datapoint 3300.[3]

Dave Gust, a CTC salesman, realized that the 2200 could meet Pillsbury Foods's need for a small computer in the field, after which the 2200 was marketed as a stand-alone computer.[3] Its industrial designer John "Jack" Frassanito has later claimed that Ray and Roche always intended the Datapoint 2200 to be a full-blown personal computer, but that they chose to keep quiet about this so as not to concern investors and others.[2][4]

The terminal's multi-chip CPU (processor)'s instruction set became the basis of the Intel 8008 instruction set, which inspired the Intel 8080 instruction set and the x86 instruction set used in the processors for the original IBM PC and its descendants.

Datapoint 2200



Datapoint 2200 computer

Manufacturer	Computer Terminal Corporation
Type	Intelligent terminal, personal computer
Release date	May 1970
Discontinued	1979[1]
Operating system	Datapoint O/S
CPU	serial, discrete logic implementation of the Intel 8008 instruction set
Memory	2 KB standard; expandable to 16 KB
Display	Text only, 80×12 characters

Technical description

The Datapoint 2200 had a built-in full-travel keyboard, a built-in 12-line, 80-column green screen monitor, and two 47 character-per-inch cassette tape drives each with 130 KB capacity. Its size, $9\frac{5}{8}$ in × $18\frac{1}{2}$ in × $19\frac{5}{8}$ in (24 cm × 47 cm × 50 cm), and shape—a box with protruding keyboard—approximated that of an IBM Selectric typewriter.[5] Initially, a Diablo 2.5 MB 2315-type removable cartridge hard disk drive was available, along with modems, several types of serial interface, parallel interface, printers and a punched card reader. Later, an 8-inch floppy disk drive was also made available, along with other, larger hard disk drives. An industry-compatible 7/9-track (user selectable) magnetic tape drive was available by 1975. In late 1977, Datapoint introduced ARCNET local area networking. The original Type 1 2200 shipped with 2 kilobytes (KiB) of serial shift register main memory, expandable to 8 KiB. The Type 2 2200 used denser 1 kbit RAM chips, giving it a default 4 KiB of memory, expandable to 16 KiB. Its starting price was around US$5,000 (equivalent to $39,000 in 2024), and a full 16 KiB Type 2 2200 had a list price of just over $14,000.

The 8-bit processor architecture that CTC designed for the Datapoint 2200 was implemented in four distinct ways, all with nearly identical instruction sets, but very different internal microarchitectures: CTC's original design that communicated data serially, CTC's parallel design, the Texas Instruments TMC 1795, and the Intel 8008.[6]

The 2200 models were succeeded by the 5500, 1100, 6600, 3800/1800, 8800, etc.

The fact that most laptops and cloud computers today store numbers in little-endian format is carried forward from the original Datapoint 2200. Because the original Datapoint 2200 had a serial processor, it needed to start with the lowest bit of the lowest byte in order to handle carries. Microprocessors descended from the Datapoint 2200 (the 8008, Z80, and the x86 chips used in most laptops and cloud computers today) kept the little-endian format used by that original Datapoint 2200.[7][8]

Datapoint 2200 version I registers

1 2	1 1	1 0	0 9	0 8	0 7	0 6	0 5	0 4	0 3	0 2	0 1	0 0	*(bit position)*
Main registers													
								A					**A**ccumulator
								B					**B** register
								C					**C** register
								D					**D** register
								E					**E** register
								H					**H** register *(indirect)*
								L					**L** register *(indirect)*
Program counter													
								P					**P**rogram **C**ounter
15-level push-down address stack													
								AS					Call level 1
								AS					Call level 2
								AS					Call level 3
								...					
								AS					Call level 13
								AS					Call level 14
								AS					Call level 15
Flags													
										C	P	Z	S Flags

Processor

The original design called for a single-chip 8-bit microprocessor for the CPU, rather than a processor built from discrete TTL modules as was conventional at the time. In 1969, CTC contracted two companies, Intel and Texas Instruments (TI), to make the chip. TI was unable to make a reliable part and dropped out. Intel was unable to make CTC's deadline. Intel and CTC renegotiated their contract, ending up with CTC keeping its money and Intel keeping the eventually completed processor.[2]

CTC released the Datapoint 2200 using about 100 TTL components (SSI/MSI chips) instead of a microprocessor, while Intel's single-chip design, eventually designated the Intel 8008, was finally released in April 1972.[9]

Possibly because of their speed advantages compared to MOS circuits, Datapoint continued to build processors out of TTL chips until the early 1980s.[7]

Nonetheless, the 8008 was to have a seminal importance. It was the basis of Intel's line of 8-bit CPUs, which was followed by their assembly language compatible 16-bit CPUs — the first members of the x86 family, as the instruction set was later to be known. Already successful and widely used, the x86 architecture's further rise after the success in 1981 of the original IBM Personal Computer with an Intel 8088 CPU means that most desktop, laptop, and server computers in use today have a CPU instruction set directly based on the work of CTC's engineers. The instruction set of the highly successful Zilog Z80 microprocessor can also be traced back to the Datapoint 2200 as the Z80 was backwards-compatible with the Intel 8080. More immediately, the Intel 8008 was adopted by very early microcomputers including the SCELBI, Mark-8, MCM/70 and Micral N.

Instruction set

Instructions are one to three bytes long, consisting of an initial opcode byte, followed by up to two bytes of operands which can be an immediate operand or a program address. Instructions operate on 8-bits only; there are no 16-bit operations. There is only one mechanism to address data memory: indirect addressing pointed to by a concatenation of the H and L registers, referenced as M. The 2200 does, however, support 13-bit program addresses. It has automatic CALL and RETURN instructions for multi-level subroutine calls and returns which can be conditionally executed, like jumps. Direct copying may be made between any two registers or a register and memory. Eight math/logic functions are supported between the accumulator (A) and any register, memory, or an immediate value. Results are always deposited in A. Most instructions are executed in 16 μs, 24 μs, or a leisurely 520 μs when accessing M. The 520 μs represents the delay of the 2200's shift register memory to fully recirculate back to the next instruction. Branch type instructions take a variable amount of time (24 μs to 520 μs) depending on the distance of the branch.

Datapoint 2200 version I instruction set

Opcode								Operands		Mnemonic	Time μs	Description
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**b2**	**b3**			
0	0	0	0	0	0	0	X	—	—	HALT	—	Halt
0	0	0	0	0	0	1	0	—	—	SLC	16	$A_{1-7} \leftarrow A_{0-6}$; $A_0 \leftarrow Cy \leftarrow A_7$
0	0	CC			0	1	1	—	—	Rcc (RETURN conditional)	16/†	If cc true, P ← (stack)
0	0	ALU			1	0	0	*data*	—	AD AC SU SB ND XR OR CP *data*	16	A ← A [ALU operation] data
0	0	DDD			1	1	0	*data*	—	Lr *data* (Load r with immediate data)	16	DDD ← data (except M)
0	0	0	0	0	1	1	1	—	—	RETURN	†	P ← (stack)
0	0	0	0	1	0	1	0	—	—	SRC	16	$A_{0-6} \leftarrow A_{1-7}$; $A_7 \leftarrow Cy \leftarrow A_0$
0	1	CC			0	0	0	*addlo*	*addhi*	Jcc *add* (JMP conditional)	24/†	If cc true, P ← add
0	1	0	0	0	0	0	1	—	—	INPUT	16	A ← input
0	1	command					1	—	—	EX *command* (external command)	16	command ← A (coded 8-31 only)
0	1	CC			0	1	0	*addlo*	*addhi*	Ccc *add* (CALL conditional)	24/†	If cc true, (stack) ← P, P ← add
0	1	0	0	0	1	0	0	*addlo*	*addhi*	JMP *add*	†	P ← add
0	1	0	0	0	1	1	0	*addlo*	*addhi*	CALL *add*	†	(stack) ← P, P ← add
1	0	ALU			SSS			—	—	ADr ACr SUr SBr NDr XRr ORr CPr	16/520	A ← A [ALU operation] SSS
1	1	0	0	0	0	0	0	—	—	NOP	16	No operation (Actually LAA)
1	1	DDD			SSS			—	—	Lds (Load d with s)	16/520	DDD ← SSS
1	1	1	1	1	1	1	1	—	—	HALT	—	Halt
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**b2**	**b3**	**Mnemonic**	**Time μs**	**Description**

SSS DDD	2	1	0	CC	ALU	
A	0	0	0	FC, C false	ADr AD (A ← A + arg)	† Variable. Can be from 24 μs to 520 μs.
B	0	0	1	FZ, Z false	ACr AC (A ← A + arg + Cy)	
C	0	1	0	FS, S false	SUr SU (A ← A - arg)	
D	0	1	1	FP, P odd	SBr SB (A ← A - arg - Cy)	
E	1	0	0	TC, C true	NDr ND (A ← A ∧ arg)	
H	1	0	1	TZ, Z true	XRr XR (A ← A ⊻ arg)	
L	1	1	0	TS, S true	ORr OR (A ← A ∨ arg)	
M	1	1	1	TP, P even	CPr CP (A - arg)	
SSS DDD	**2**	**1**	**0**	**CC**	**ALU**	

Performance

Although the Datapoint 2200 version I is somewhat faster than an Intel 8008 on register instructions, any reference to the 2200's shift-register memory incurs a large 520 µs delay. Also any JMP, CALL, or RETURN can incur a variable delay up to 520 µs depending on the distance to the new address. The parallel-architecture Datapoint 2200 version II is much faster than either.[5][10]

Instruction	Description	Datapoint 2200 ver I µs	500 kHz Intel 8008 µs	Datapoint 2200 ver II µs
ADB	Add B to A	16	20	3.2
ADI nn	Add nn immediate to A	16	32	4.8
ADM	Add memory to A	520	32	4.8
JMP nnnn	Jump to nnnn	24-520	44	6.4
CALL+RET	Call and Ret combined	520	64	9.6
Rcc (false)	Conditional return not taken	16	12	3.2

Code example

The following Datapoint 2200 assembly source code is for a subroutine named MEMCPY that copies a block of data bytes from one location to another. Because the byte counter is only 8 bits, there is enough room to load all the subroutine parameters into the 2200's register file. Datapoint 2200 version I transfers 374 bytes per second using this routine. A 500 kHz Intel 8008 executes this code almost four times faster, transferring 1,479 bytes per second. Datapoint 2200 version II is much faster than either at 9,615 bytes per second.[5][10] If more than an 8-bit count is needed, a more complicated copy routine with parameters held in memory would be required.

```
                                ; MEMCPY --
                                ; Copy a block of memory from one location to another
                                ;
                                ; Entry parameters in registers
                                ;       HL: 13-bit address of source data block
                                ;       DE: 13-bit address of target data block
                                ;       C: 8-bit count of bytes to copy. (1 to 256 bytes)

                                        ORG     2000Q       ;Code at 002000 octal
002000  317             MEMCPY  LBM                 ;Read source byte into B
002001  206 020 004             CALL    XCHGI       ;Exchange HL<->DE and increment DE
002004  371                     LMB                 ;Save B to target byte
002005  206 020 004             CALL    XCHGI       ;Exchange HL<->DE and increment DE
002010  302                     LAC                 ;Decrement byte counter in C
002011  024 001                 SU      1
002013  320                     LCA
002014  110 000 004             JFZ     MEMCPY     ;Continue for all bytes
002017  007                     RETURN

                                ;Exchange DE and HL register pairs then increment DE as 16 bits
002020  306             XCHGI   LAL                 ;Exchange L and E
002021  364                     LLE
002022  004 001                 AD      1           ;and inc E, low byte of DE
002024  340                     LEA
002025  305                     LAH                 ;Exchange H and D
002026  353                     LHD
002027  014 000                 AC      0           ;proagate Cy into D
002031  330                     LDA
002032  007                     RETURN
002032                          END
```

Credits

The original instruction set architecture was developed by Victor Poor and Harry Pyle.[11] The TTL design they ended up using was made by Gary Asbell. Industrial design (how the box's exterior looked, including the company's logo) was done by Jack Frassanito.[2]

Specifications

Main unit

- Processor: 8-bit CPU instruction set architecture with a bit-serial microarchitecture assembled from standard TTL components.
- Memory: 2K byte shift register memory, expandable to 8K (Version II: 4K RAM, expandable to 16K)
- Display: Text only, 80×12 characters
- Storage: 2 tape drives, optional 8-inch Shugart floppy drive

Peripherals

Users of the 2200 and succeeding terminals eventually had several optional units to choose from. Among these were:

- Modems
- Hard disks

- Printers
- ARCnet LAN

See also

- Sycor 302, a programmable terminal introduced in 1969 with similar characteristics to the 2200
- Kenbak-1

References

1. "Datapoint Corporation Datapoint 2200" (https://www.old-computers.com/museum/computer.asp?c=596). *OLD-COMPUTERS.COM : The Museum*.
2. Wood, Lamont (August 8, 2008). "Forgotten PC history: The true origins of the personal computer" (https://www.computerworld.com/article/2532590/forgotten-pc-history--the-true-origins-of-the-personal-computer.html). *Computerworld*.
3. Wood, Lamont (2013). *Datapoint: The Lost Story of the Texans Who Invented the Personal Computer* (https://books.google.com/books?id=idTeAAAAQBAJ&pg=PT102). Hugo House Publishers, Ltd. pp. 102–103. ISBN 9781936449361.
4. Weinkrantz, Allen (June 2, 2009). "San Antonio Has Claim As The Birthplace of the Personal Computer. Read All About It" (https://web.archive.org/web/20160304040904/http://www.alanweinkrantz.com/san-antonio-has-claim-as-the-birthplace-of-the-personal-computer-read-all-about-it/). Archived from the original (http://www.alanweinkrantz.com/san-antonio-has-claim-as-the-birthplace-of-the-personal-computer-read-all-about-it/) on March 4, 2016.
5. *Datapoint 2200 Reference* (http://www.bitsavers.org/pdf/datapoint/2200/2200_Reference_Manual.pdf) (PDF). Computer Terminal Corporation. 1972. Retrieved September 16, 2024.
6. Shirriff, Ken (August 30, 2016). "The Surprising Story of the First Microprocessors" (https://spectrum.ieee.org/the-surprising-story-of-the-first-microprocessors). *IEEE Spectrum*. **53** (9): 48–54. doi:10.1109/MSPEC.2016.7551353 (https://doi.org/10.1109%2FMSPEC.2016.7551353). S2CID 32003640 (https://api.semanticscholar.org/CorpusID:32003640).
7. Shirriff, Ken. "The Texas Instruments TMX 1795: the first, forgotten microprocessor" (https://www.righto.com/2015/05/the-texas-instruments-tmx-1795-first.html).
8. "Oral History Panel on the Development and Promotion of the Intel 8008 Microprocessor" (http://archive.computerhistory.org/resources/text/Oral_History/Intel_8008/Intel_8008_1.oral_history.2006.102657982.pdf) (PDF). September 21, 2006. p. 5.
9. Thompson Kaye, Glynnis (1984). *A Revolution in Progress - A History to Date of Intel* (https://www.intel.com/Assets/PDF/General/15yrs.pdf) (PDF). Intel Corporation. p. 13. "The 8-bit 8008 microprocessor had been developed in tandem with the 4004 and was introduced in April 1972. It was originally intended to be a custom chip for Computer Terminals Corp. of Texas, later to be known as Datapoint." "As it developed, CTC rejected the 8008 because it was too slow for the company's purpose and required too many supporting chips."
10. *8008 8 Bit Parallel Central Processor Unit* (http://www.bitsavers.org/components/intel/MCS8/Intel_8008_8-Bit_Parallel_Central_Processing_Unit_Rev4_Nov73.pdf) (PDF) (Rev 4, Second Printing ed.). Intel. November 1973. pp. 14, 17. Retrieved April 30, 2024.
11. Dalakov, Georgi (April 23, 2014). "History of Computers and Computing, Birth of the modern computer, Personal computer, Datapoint 2200" (http://history-computer.com/ModernComputer/Personal/Datapoint.html).

External links

- Information about the Datapoint 2200 at OLD-COMPUTERS.COM (https://www.old-computers.com/museum/computer.asp?st=1&c=596) – Including a picture of the terminal
- Datapoint documentation (http://bitsavers.org/pdf/datapoint/2200/) on bitsavers.org
- Page with links to a doctoral thesis about early microprocessor history, with many details about Datapoint's role (https://web.archive.org/web/20061219012629/http://home.comcast.net/~gordonepeterson2/schaller_dissertation_2004.pdf)
- The man who invented the PC (https://www.inventionandtech.com/content/man-who-invented-pc-1)
- datapoint.org: Unofficial Datapoint Organization WEB site (http://www.datapoint.org)