THE◆BRIDGE

The Magazine of Eta Kappa Nu

AUTUMN 2010
vol. 106 / no. 1

Shining a light on
Electronic Design in the 21st Century

FEATURES

Designing a Multilayer PCB Stack-up

High-Speed Serial Signaling

Challenges – An Interview with Dr. Howard Johnson

HKN

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LETTER FROM THE EXECUTIVE DIRECTOR

Fern E. Katronetsky | Eta Chapter Member

Dear HKN Members:

The end of a year always provides an opportunity to review the year's accomplishments and develop plans for the future. As we look back on 2010, we see many accomplishments of which all HKN members should be proud.

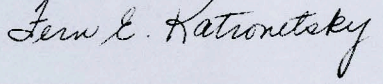
The awards program continues to recognize the outstanding achievements of HKN members and professionals in the community who have made important contributions to industry and society as a whole. Two new Eminent Members, one Karapetoff award winner, an outstanding teacher and student, and a record 22 outstanding chapters have been recognized in the last year. Please continue to nominate the deserving individuals with whom you are acquainted for an award.

A very successful HKN student leadership conference was hosted by Beta Xi chapter at the University of Oklahoma in November 2010. Students had ample opportunity to network with each other and industry representatives. Distinguished speakers were invited and the many chapters that were in attendance enjoyed a weekend of leadership activities, teamwork development, education and fun. We thank the sponsoring organizations, and the generous HKN alumni, who made this conference possible. We plan to continue with these student leadership conferences as we move into 2011. Be sure to submit your chapter's application for consideration in holding the next event.

Finally, we can say that the merger between HKN and IEEE is complete. As IEEE-HKN, we are in a stronger position to sustain the interest and commitment of our members by being active alumni. And through IEEE's global presence in industry, the IEEE-HKN image will be the epitome of engineering leadership excellence. Not only do we get to have these things, but we also get to have a permanent corporate "home."

Thank you for your continued support of HKN. We hope you enjoy this issue of *THE BRIDGE*.

Best wishes,



LETTER FROM THE EDITOR

Barry J. Sullivan | Beta Omicron Chapter Member

Mention electronic design and you will conjure up images of integrated circuits and the intricate layouts of the chips that lie at heart of so many modern consumer and industrial products. What goes on around and between the chips is just as important to a successful electronic product as what happens inside them, however.

This issue of *THE BRIDGE* recognizes the challenges faced by those who design with chips, as well as those who design the chips themselves. The first article in particular illustrates the complexity of printed-circuit board design, which requires more than simply arranging and connecting devices in two dimensions.

The field of signal integrity is concerned with maintaining the fidelity of information carried by a signal as it traverses chips, boards, and cables between the transmitting and receiving devices. Designs that push the information-bearing capability of signals need methods for validating their integrity, which is the topic of the second article. Finally, a profile of a leading signal integrity expert shows that this is a discipline that can be practiced in the mountains of Washington State as well as in Silicon Valley.

We encourage HKN members to suggest topics and share their experiences through full-length articles and member profiles. If you are interested in contributing an article or a profile, please direct your inquiries to *editor@hkn.org*.

Warm regards,

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Autumn 2010

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Eta Kappa Nu (HKN) was founded by Maurice L. Carr at the University of Illinois on October 28, 1904, to encourage excellence in education for the benefit of the public. HKN fosters excellence by recognizing those students and professionals who have conferred honor upon engineering education through distinguished scholarship, activities, leadership, and exemplary character as students in electrical or computer engineering or by their professional attainments.

THE BRIDGE is the official publication of the Eta Kappa Nu Association.

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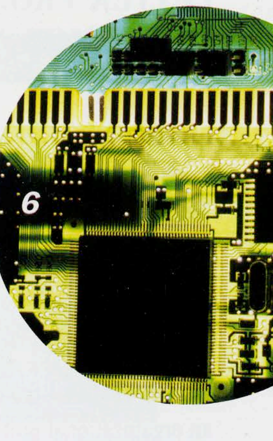
ISSN-0006-0809 vol. 106 / no. 1

The Magazine of Eta Kappa Nu

features



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Printed-circuit boards (PCBs) appear to the casual observer as merely a way to anchor and interconnect sophisticated electronic components. This article demonstrates that PCBs are themselves complex structures requiring careful specification to support the signaling speeds typical of many electronic designs.

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by Ransom Stephens and John Calvin

Designs that push limits of data transfer and enable high-speed communication between devices need state-of-the-art tools and techniques to verify the integrity of signals sent from one device to the next: A "receiver tolerance test" measures the ability of receiving device to successfully recover a corrupted signal and illustrates the challenges encountered in designing advanced digital electronics.

14 Challenges – An Interview with Dr. Howard Johnson

Howard Johnson is a leading authority in signal integrity and high-performance digital electronic design. As this profile shows, he has found a way to practice his chosen profession in surroundings quite different from the cubical stereotype of the engineering workplace.

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LETTER FROM THE PRESIDENT

Bruce Eisenstein | HKN President

IEEE-HKN Merger Complete

It's Official! On 1 September 2010, the merger of HKN with IEEE was completed. We have now officially become IEEE-HKN, and are an organizational unit of IEEE. But we will continue to be run as we have been, that is, by our Board of Governors. The Board of Governors of IEEE-HKN will be responsible for Eta Kappa Nu's customs and rituals, criteria for membership, managing IEEE-HKN's resources, and administering and hosting IEEE-HKN's on-line presence.

As I mentioned in the Spring 2009 issue of THE BRIDGE, chapter/branch relationships will remain unchanged and are being left to the local wisdom. What will change is that Chapter Bylaws will need to be modified to reflect the fields of interest of IEEE, and not just focus on electrical and computer engineering. In addition, those wishing to establish Chapters will need to do the same—broaden the scope to the fields of interest of IEEE.

The "new" IEEE-HKN Board of Governors held its first meeting in mid-November since the completion of the merger. It was reported at this meeting that the $1.2 million that IEEE agreed to deposit upon merger was transferred into an IEEE-HKN restricted account held by the IEEE Foundation. The funds held by HKN were also transferred to the same restricted account. Over the last several years, the Board of Governors has come to realize that its induction fee for members into HKN, which has not changed in almost 20 years, needed to be revisited. It was the decision of the Board of Governors, at its November meeting, to increase its induction fee to $50 effective 1 January 2011. In addition, the induction fee will continue to be reviewed on an annual basis.

The annual election results of the active voting Chapters are in. The incoming President for 2011 is Dr. Stephen M. Goodnick. Dr. Goodnick currently sits on the IEEE-HKN Board of Governors as its Vice President and, as President, has been elected for a one-year term. He is Professor, School of Electrical Computer and Energy Engineering and is Director, Arizona Initiative for Renewable Energy, at Arizona State University. The incoming Vice President for 2011 is Dr. John A. Orr. Dr. Orr previously served as a member of the Board of Governors. He is currently Professor, ECE at Worcester Polytechnic Institute, and served as its Provost until June, 2010. Also elected were Dr. W. Kenneth Jenkins, Professor of EE and Department Head at The Pennsylvania State University as Governor East—Region, and Dr. H. Vincent Poor, Dean, School of Engineering and Applied Science, Michael Henry Strater University Professor of Electrical Engineering at Princeton University as Governor at Large.

I have had the pleasure of serving as your President for the last three and one-half years, and am happy to have witnessed the merger between IEEE and HKN. It is exciting to know that HKN will continue to exist as the student honor society it was meant to be and that its expansion around the world will benefit HKN members now and in the future.

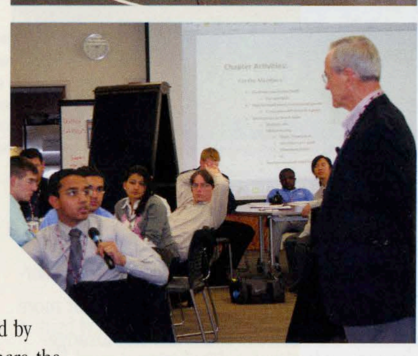
I would like to take this opportunity to thank all of you for allowing me to serve as your president.

Bruce A. Eisenstein

2010 HKN Student Leadership Conference

This year, more than 60 HKN student members from chapters across the country gathered at the University of Oklahoma November 5-7, 2010 for a weekend conference hosted and organized by the Beta Xi chapter. This year's conference theme was "Engineering in a Multidisciplinary World."

The pre-conference activities began on Friday with a special LabVIEW NXT Training Session, hosted by National Instruments. The software provided the platform for the weekend's team building project – building and programming Sumo Bots for a final competition to be held at the end of the weekend.



Saturday morning, the conference began with a welcome from Dr. Simin Pulat, Associate Dean for Undergraduate Programs at OU. HKN Board of Governors members Stephen Goodnick and Evelyn Hirt also welcomed members and discussed the recent IEEE-HKN merger with students.

Students later enjoyed a lecture by Dave Wilson of National Instruments who provided an overview of National Instruments' recent initiatives. Students then participated in several hands on demos utilizing National Instruments' technologies for a fun and interactive session.

The chapter development workshop, a crucial component of the student conference agenda, was moderated by M-Gen Jerry Holmes, USAF Retiree, who led a thought-provoking session for students allowing them to share the activities and ideas from their respective chapters. Students came away with new ideas for fundraising, chapter activities, and recruiting and initiation.

Later in the afternoon, Tom Walker of I2E spoke about the opportunities available when working with a startup company. He answered a variety of questions about what to look for when exploring employment opportunities in this area while exposing students to a new avenue to consider.

The evening concluded with a visit to the University of Oklahoma's National Weather Center for a tour of the facility, dinner, and keynote by Dr. Pam Heinselman, NOAA.

HKN would like to extend a special thank you to the University of Oklahoma, National Instruments, the OU College of Engineering, OU Electrical and Computer Engineering, and the Oklahoma Center for the Advancement of Science and Technology for sponsoring the activities of the conference. Without their support, Beta Xi would not have been able to organize and conduct such a successful event.

If your university is interested in hosting a future conference, please contact headquarters at **info@hkn.org** for more information about how to submit a proposal.

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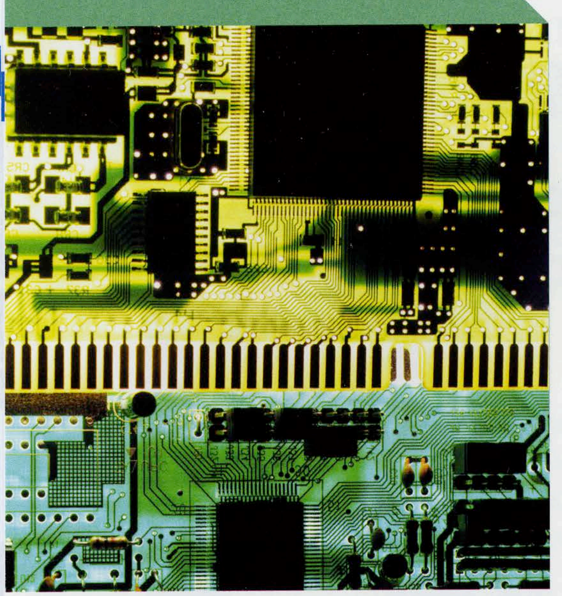


Designing a Multilayer PCB Stack-up

by Lee Ritchey

Signaling speeds on printed-circuit boards (PCBs) have increased to the point where signal integrity and power delivery considerations make it necessary to employ far more discipline in the choice of materials and arrangement of the layers in the stack-up—both of which are outside the skill-set of virtually all PCB fabricators. The common practice of leaving the vital PCB stack-up design in the hands of PCB fabrication engineers carries with it significant hazards. It is often the case that the only criteria given to a fabricator is the overall number of layers, desired total thickness and expected impedance of the transmission lines. This method of arriving at a PCB stack-up can result in a different PCB from every fabricator who quotes on the job as well as significant signal integrity risks.

How a Typical Multilayer PCB Is Built

In order to understand the choices that must be made when designing a PCB stack-up, it is useful to review how a typical multilayer PCB is fabricated. Figure 1 is a diagram showing the components that make up a six-layer PCB. The manufacturing method shown in the figure is referred to as foil lamination. This refers to the fact that the two outer layers begin as sheets of foil copper with no images etched into them. This is the most cost effective way there is to manufacture a multilayer PCB and should be the objective of the stack-up design process. There are other methods available, such as "cap" lamination that forms the outer layers as part of a two-sided piece of laminate and "build up" processing that involves blind and buried vias. These choices always result in more expensive PCBs and should be considered only as a last resort.

It should be noted that PCB layers are built in pairs. Therefore, PCBs normally have an even number of layers. As a result, when additional layers are needed they will be added one pair at a time along with an additional pre-preg layer. Designing a stack-up with an odd number of layers when only one additional layer is needed does not result in a cheaper PCB than if a pair of layers is added. The reason for this is the fabricator will need to purchase a piece of laminate for the added layer that has copper foil on both sides. The copper foil that is not needed will be etched away when the foil side that is needed is etched.

As can be seen from Figure 1, three main components make up a multilayer PCB. These are:

- Sheets of laminate that have a sheet of copper foil bonded to each side which have the patterns for either signal layers or plane layers etched into the copper foils. These are often referred to as "details". (Laminate is a combination of woven glass cloth and a resin system such as epoxy or polyimide.) The thickness of the copper on each side of this laminate can vary from ½ ounce to 2 ounces. (Copper foil thickness is specified in ounces per square foot of surface area. 1 ounce is approximately 1.4 mil or 36 microns thick.)
- Sheets of uncured laminate called pre-preg placed between the details and between details and the outer foil sheets. This pre-preg is woven glass material coated with the same resin system that is used in the laminates. Unlike the laminates, the resin is only partially cured. During lamination heat will cause this resin to melt and flow into the voids in the adjacent copper layers, serving as the "glue" to bond the layers together and then cure it to the same rigid state as the resin in the laminate. After lamination pre-preg is indistinguishable from laminate.
- Sheets of copper foil to form the outer layers. The reason the two outer layers are solid copper at this stage instead of etched with the outer layer patterns is to provide a path for the current required to plate copper into the holes drilled through the PCB for vias and component leads.

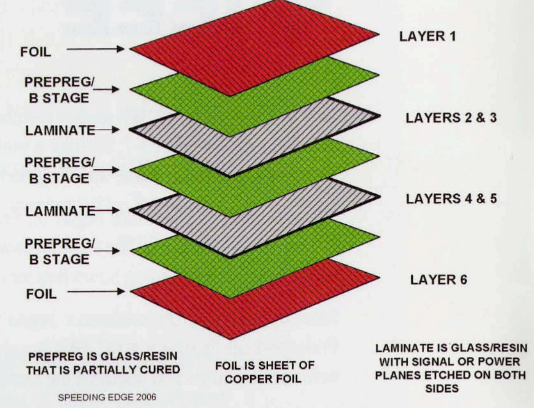


Figure 1 *A Typical Six-Layer PCB Stack-Up Using Foil Lamination*

The task of the stack-up designer is to select combinations of pre-preg, laminate and foils that provide the desired electrical characteristics while satisfying cost and manufacturability goals.

Alternative PCB Fabrication Methods

Figure 2 is an illustration of the "cap" lamination method of manufacturing a multilayer PCB. As can be seen, there are three pieces of laminate each with two conductor layers in this version of a six-layer PCB. The most obvious difference between this and foil lamination for this six-layer PCB is that only two pieces of laminate or details must be processed using foil lamination while three are required with cap lamination. This represents a cost increase over foil lamination. This was the method used to fabricate PCBs in the early days of multilayer PCB fabrication.

A third method for creating a multilayer PCB is by the use of buried and blind vias. In one version of this method, the internal n-2 layers are fabricated using either of the two methods shown above resulting in a complete sub-PCB with plated through holes running from layer 2 to layer n-1. Then, a piece of pre-preg and a piece of foil are added to each side and the combination is laminated into a final PCB of n layers. After this second lamination step, holes are drilled through the entire stack-up and plated. It is also common to drill blind vias from layer 1 to layer 2 and layer n to layer n-1 as well. It is easy to see that this method will result in a significantly more expensive PCB that takes longer to manufacture than either of the above choices. (In some cases PCBs designed to use buried vias can cost as much as twice what the same number of layers would cost using only through-hole vias.)

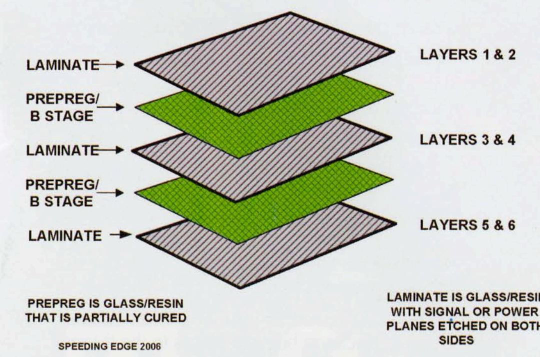
Types of Signal Layers

Figure 3 is a typical ten-layer PCB stack-up. This example has three types of signal layers. They are: surface microstrip (L1 & L10), buried microstrip (L2 and L9) and off-center or dual stripline (L5 & L6).

There is a fourth type of signal layer: centered or symmetrical stripline, which is a single stripline layer centered between two planes. The reason that dual stripline is used more often than single stripline is that each time a single stripline layer is added to a stack-up a plane must also be added to isolate signal layers from each other resulting in higher layer counts for a given number of signal layers. The method used to keep the two signal layers in the dual stripline configuration from interfering with each other (crosstalk) is to route signals on one layer horizontal and on the other vertical.

In this example, the two outer layers are not used for signals. The reason is impedance uniformity on these layers is difficult to control accurately due to the uneven plating of copper that often results when plating is done to plate copper in the holes that conduct current such as vias and power leads.

Figure 2 *Typical Six-Layer PCB Using Cap Lamination*



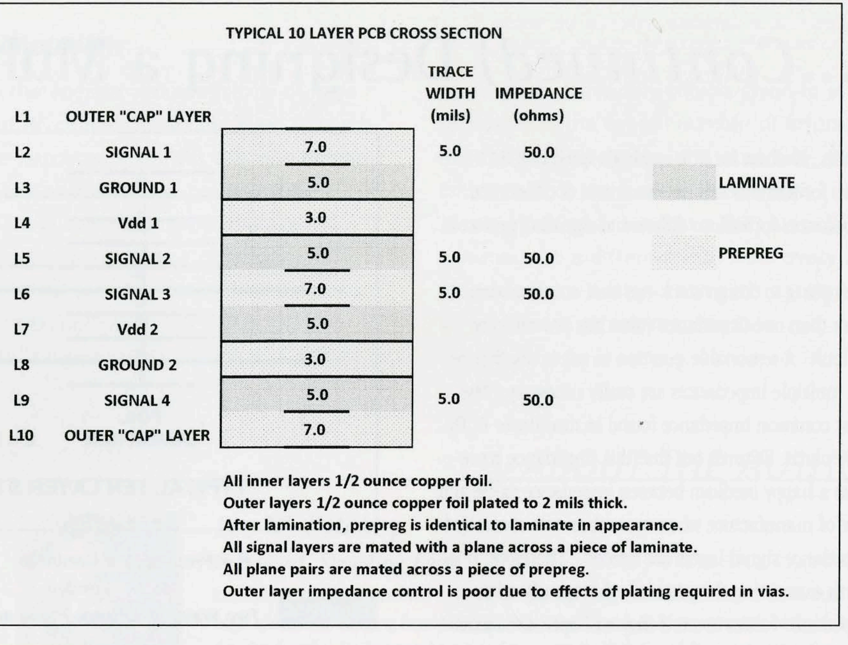


Figure 3 *A Typical 10-Layer PCB Stack-Up*

Alternate Ways to Stack Layers

Figure 4 shows two different ways to arrange the layers in a ten-layer PCB. The short bars represent signal layers and the long bars represent planes. The stacking on the left appears to have two more signal layers than the one on the right due to the fact that the top and bottom layers on the right are not available for signals and this is true. The disadvantages of the stack-up on the left are power-delivery related. Most high-speed designs require plane capacitance to support fast switching edges. In order to create plane capacitance, pairs of planes must be close to each other (less than 4 mils, 100 microns). The stack-up on the left has only one plane pair close together while the stack-up on the right has two plane pairs.

A second benefit of the stack-up on the right is that the plane pairs are separated by pre-preg which can be made very thin, less than 3 mils, as shown in Figure 3. This is of significant value when designing a power delivery system.

A third benefit of the stack-up on the right is that each signal layer is paired with a power plane across a piece of laminate. The benefit here is that during lamination, the thickness of the laminate does not change and this makes it possible to achieve tightly controlled impedances on the transmission lines. When a signal layer is mated with a plane across a piece of pre-preg, impedance control is more difficult as the pre-preg thickness can change significantly during the press cycle.

For all the reasons given above, the layer stacking on the right represents the best compromise between power delivery and impedance accuracy. If two more signal layers are needed, they would be added along with two more planes resulting in a 14-layer PCB. If four more signal layers are needed then four more signal and four more plane layers would be added resulting in an 18-layer PCB and so on for 22 and 26 layers.

Selecting an Impedance

The starting point for most PCB stack-up design is determining what impedance or impedances to use in each signal layer. A number of impedances have been used for controlled impedance PCBs. Among these are 62 or 65 ohms for PCI buses, 72 or 75 ohms for video

Continued on next page...

(...Continued) Designing a Multilayer PCB Stack-up

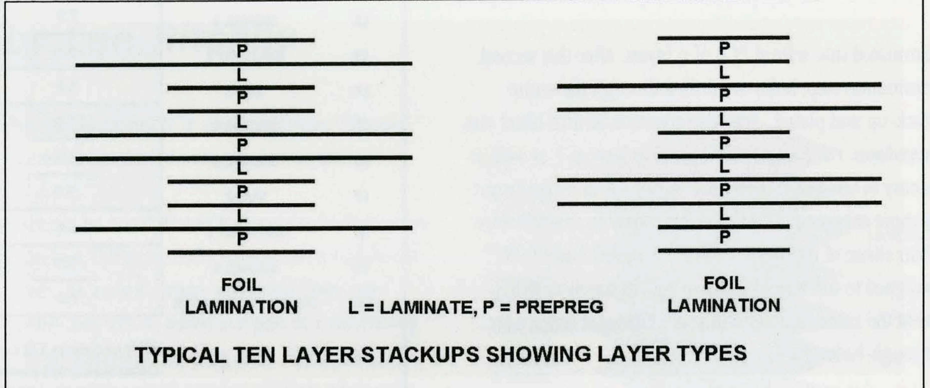
signals, 50 ohms for ECL and high speed CMOS, 28 ohms for Rambus and an assortment of differential impedances for various differential signaling protocols.

Attempting to design stack-ups that accommodate more than one impedance value has proven to be difficult. A reasonable question to ask is whether or not multiple impedances are really necessary. The most common impedance found in multilayer PCBs is 50 ohms. It turns out that this impedance represents a happy medium between impedance value and ease of manufacture when more than two controlled impedance signal layers are needed. Therefore, it is worth examining the protocols that specify other impedance values to see if they will operate successfully with a 50-ohm transmission line.

An impedance of 50 ohms is achieved on stripline layers with a trace width that is about the same as the dielectric thickness. In order to make a 62-ohm line for the PCI bus the trace width has to be made very narrow in stripline layers. A similar analysis will show that the Rambus protocol also works properly with 50-ohm transmission lines. (To make a 28-ohm line the trace width must be so wide that it will not fit between pins on a BGA.)

This leaves 72-ohm video and the various differential protocols. In almost all cases, the 72-ohm video requirement is to match 72-ohm coaxial cable bringing a signal onto a PCB or taking it off the PCB. Building a stack-up that allows both 50 ohms and 72 ohms in the same signal layer is very difficult, if not impossible. Is that really necessary? I have found that if the IC using the video signal is located close to the edge of the PCB, as most are, a very short trace of 50 ohms is not going to significantly degrade the video signal. This can be easily validated using any good SI simulator.

The 100-ohm differential impedance requirement is an artifact of the need to provide two 50-ohm lines each parallel terminated in 50 ohms. The optimum way to route differential signals in a PCB is so that each member of a pair does not interact with the other. This is achieved by separating them from each other far enough so that one does not drive down the impedance of the other. When this is done, it is no longer necessary to specify differential impedance. As



P = Prepreg L = Laminate

Figure 4 ***Two Ways to Arrange Plane and Signal Layers in a 10-Layer PCB***

a result, all of the signals that need controlled impedance can be routed with the same impedance.

From all of this, it can be seen that 50 ohms is a very good compromise impedance. It also happens to be in the "sweet spot" of the PCB fabrication process as well as of all the tools used to measure impedance and other characteristics of transmission lines. Therefore, it is wise to construct stack-ups that have a nominal impedance of 50 ohms.

In spite of what might be called out in some applications notes, every modern logic family fast enough to require controlled impedance and terminations is capable of driving a 50-ohm transmission line so there is no need to design complex stack-ups that require complex routing rules in order to make all of the nets fit into the space available in the signal layers.

Selecting Laminates

PCB material systems are defined by the resin systems used to make the laminate and prepreg. To a lesser extent the type of glass is also part of how a laminate system is differentiated from its competition. For the most part, a glass composition known as "E" glass is used.

There are a number of properties of laminates that must be taken into account when selecting a laminate system. Among these are:

- Does the PCB require lead-free assembly?
- Does the PCB require a high Tg (ability to withstand high temperatures)
- Does the design require a low loss laminate?
- Can the program tolerate a single-source laminate?
- Will production volumes be manufactured in a different shop or country than the prototypes?

When most of these conditions must be met, many laminate types will be eliminated from consideration.

Steps in Designing a Stack-Up

From all of the above discussion, designing a proper PCB stack-up might be a bit confusing. These are the steps I go through when designing a stack-up. I prefer the stack-up approach shown on the right side of Figure 4 when the number of signal layers is beyond 2. Here are the steps I take:

1. Set the height of the signal layers above their plane partners as thin as is practical to yield good manufacturing results. This is 3 or 4 mils (76 or 102 microns) for most good fabricators.
2. Choose copper thickness for each layer that meets the signal integrity needs and is easy to manufacture.
3. Choose a glass style for these pieces of laminate that will result in uniform impedance and good differential pair performance at high data rates.
4. Set the trace width to yield the proper impedance.
5. Set the trace-to-trace separation to meet crosstalk goals.
6. Set the thickness between planes to the thinnest prepreg that will result in good yields. (Thin is good for power delivery, meaning high interplane capacitance.)
7. Set the thickness between signal layers and between L2 and the surface and Ln-2 and the surface to meet the overall thickness goal. (Variations in the thickness of these pieces of prepreg have an effect on trace impedance, but it is far smaller than variations in the thickness of the laminate between the trace layers and their nearest planes.)

Once the laminate and prepreg choices have been made that meet all of the goals, these must be recorded on the stack-up drawing so that multiple fabricators don't build different PCBs. For example, one manufacturer offers three different choices for a 4-mil piece of laminate and three for 5 mils. The properties of these can be quite different, so listing only 4-mil or 5-mil dimensions on the stack-up drawing is not enough to guarantee two fabricators will build the board the same way. I have had a number of students in my classes who were there because the fabricator was changed from prototyping to production and the production PCBs did not work. On investigation, it was determined that each fabricator used different laminate all of the same thickness.

Conclusion

As the speeds and complexity of logic and RF circuits have continued to climb, the importance of PCB stack-up design in the overall design process has become more and more important. The common practice of leaving the vital PCB stack-up design in the hands of PCB fabrication engineers carries with it significant hazards. It is often the case that the only criteria given to a fabricator is the overall number of layers, desired total thickness and expected impedance of the transmission lines. This method of arriving at a PCB stackup can result in a different PCB from every fabricator who quotes on the job as well as significant signal integrity risks.

ABOUT THE AUTHOR

Lee W. Ritchey

President, Speeding Edge

Lee Ritchey has been involved in or supervised the design and fabrication of more than 3000 high speed PCBs ranging from video game mother boards to supercomputer backplanes and daughter cards. He has taught a two day course in High Speed Design to more than 7000 engineers around the world and has authored two text books on the subject "Right The First Time, A Practical Handbook On High Speed PCB And System Design, Volumes 1 and 2". He has also written numerous articles on PCB design and fabrication and is currently a regular columnist for Circuitree magazine. He has been instrumental in the development of the two leading PCB stack-up design tools. Mr. Ritchey has a BSEE degree from California State University at Sacramento with a specialty in microwave engineering. He has worked on programs ranging from the Apollo Mission to some of the largest supercomputers in the world.

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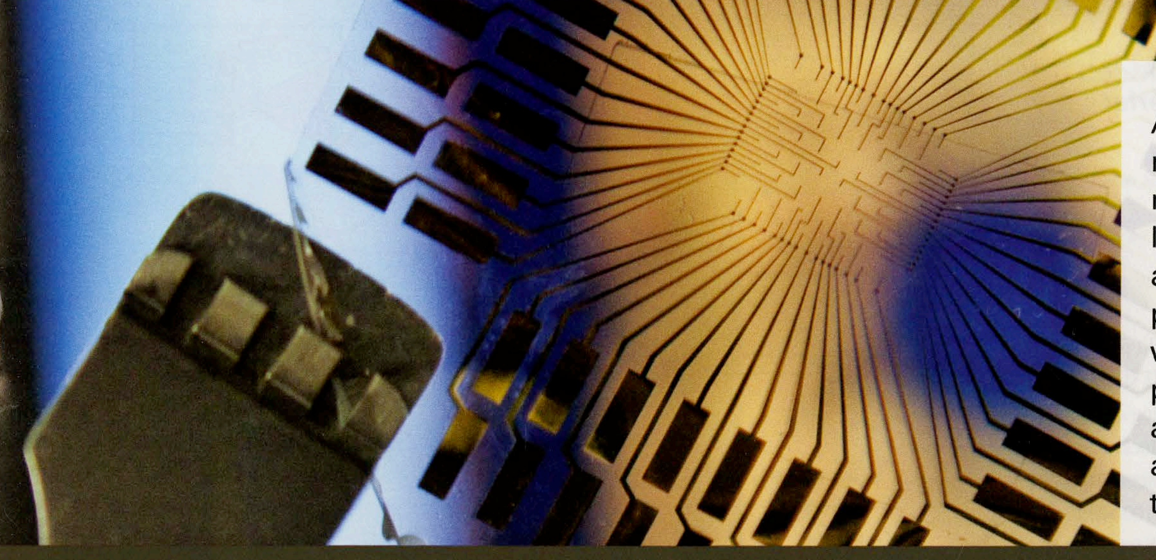

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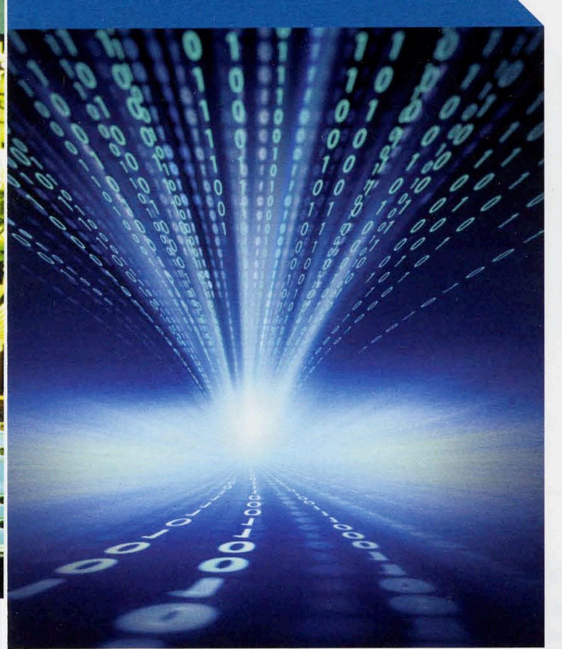

High-Speed Serial Signaling

by Ransom Stephens and John Calvin

The successful operation of links at multi-gigabit-per-second data rates requires either an extraordinarily high quality transmission path or a receiver architecture capable of tolerating crosstalk, jitter, and amplitude noise. Over the last decade, communications and computer standards such as PCI Express, Serial ATA and 10 Gigabit Ethernet increasingly require that receivers include components that enable them to tolerate impairments. Clock data recovery and equalization circuits allow receivers to accommodate signals that may be so distorted that they are unrecognizable as digital signals.

Review of High-Speed Serial Technology

Figure 1 shows the standard components of a serial data system.

The transmitter – serializer, reference clock and multiplier

Starting on the left end of Figure 1, eight parallel inputs are multiplexed into a serial data stream. At the transmitter, timing of the serial logic transitions is governed by a reference clock. The reference clock, which might be synthesized or based on a crystal oscillator usually at 100 MHz, is multiplied up to the data rate by a Phase Locked Loop (PLL).

Most of the emerging serial data standards include an option for Spread Spectrum Clocking (SSC). SSC is low frequency modulation of the clock which spreads the radiated energy of the system over a larger frequency band and makes it easier for the transmitter to pass government electromagnetic interference regulations. The most common form of SSC is 33-kHz triangle-wave frequency modulation with amplitude of a few thousand parts per million.

The primary sources of signal degradation at the transmitter are:

(1) Phase noise of the reference clock, which increases as the square of the multiplication factor of the PLL and is the primary random jitter (RJ) source.

(2) Duty Cycle Distortion (DCD) caused by skew in the parallel input stream and/or asymmetry in the duration of adjacent clock cycles. The result is a difference in the duration of high and low logic levels. DCD doesn't combine linearly with other signal degradations.

The transmission path – backplanes and cables

The serialized data then propagates along a transmission path to the receiver. Differential signaling is almost always used to reduce stray fields and crosstalk – the net electromagnetic radiation of two neighboring transmission paths, each transmitting the opposite waveform, is very nearly zero, even when there is a common mode voltage.

The transmission path may include both Printed Circuit Board (PCB) and cables. Circuit boards and backplanes are usually made of Flame Retardant Type 4 fiberglass weave (FR-4). The cables might be high quality matched cables, but are more likely twisted pair. Figure 2 shows the progressive impairment of a signal as it traverses increasing lengths of transmission paths. The same thing happens as the data rate increases; inter-symbol interference (ISI) rapidly degrades a pristine digital signal into a nasty looking waveform (Figure 3).

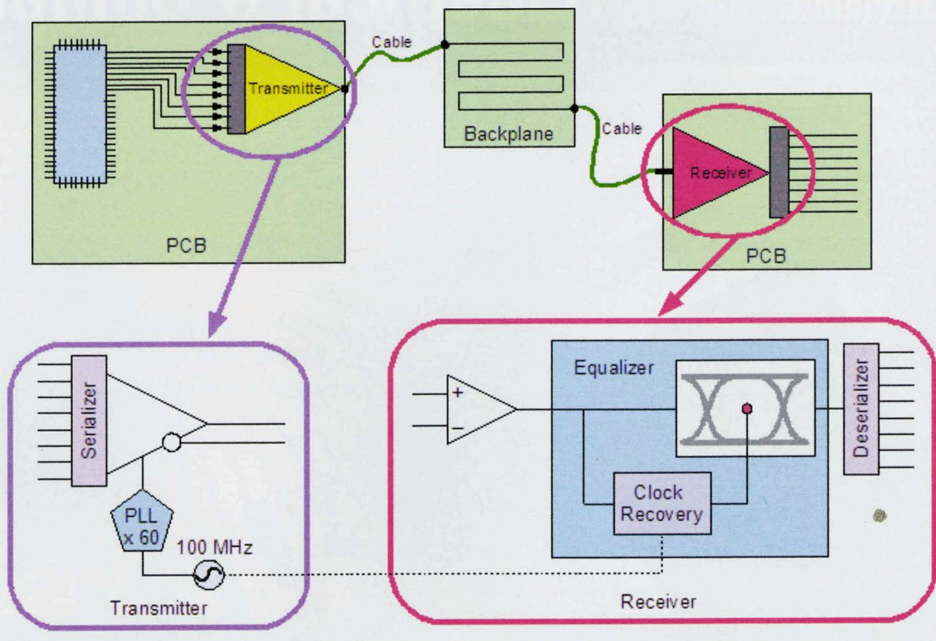

Figure 1 *Serial data straw diagram.*

EyeAWG Waveform Synthesis Fidelity: Progressive Impairment of a SATA Gen3 (6Gb/sec) Lone Bit Pattern

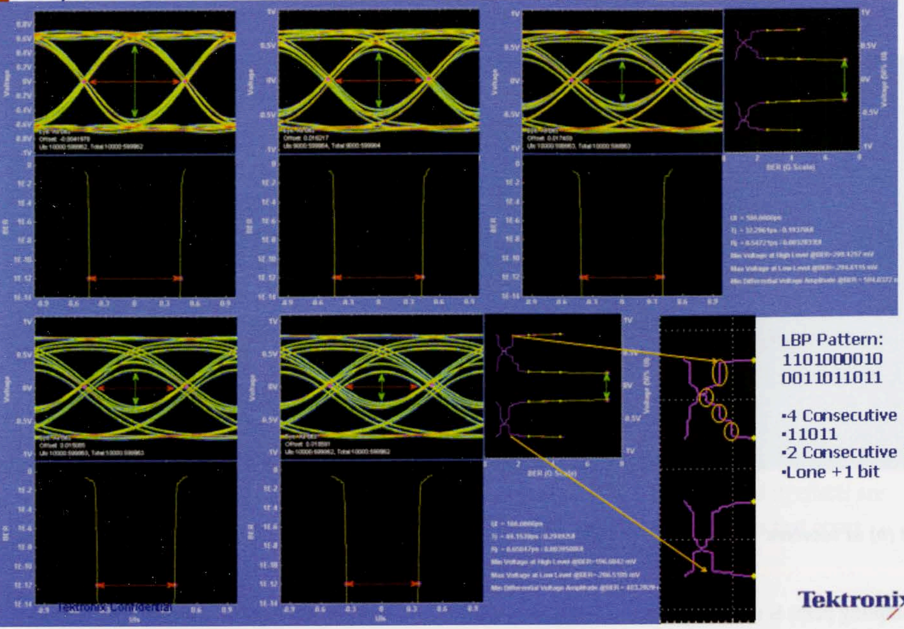

Figure 2 *From left to right and top to bottom, the progressive impairment of a signal as it traverses successively longer transmission paths.*

The resistance of the conductor causes signal attenuation; the skin effect and dispersion cause non-uniform frequency response. The dominant frequency component of a given bit is determined by the bit pattern that immediately surrounds it. In Figure 4, a simple Resistor-Capacitor (RC) time constant is used to illustrate ISI. In the top trace—where the data signal, 01010101, is a clock signal at half the data rate—the response of the circuit is sufficient for each bit to cross the logic-decision voltage threshold and be accurately identified. In the middle trace, the data signal, 00001111, is a clock signal at one-eighth the data rate. Over the string of Consecutive Identical Bits (CIB or CID) the time constant is sufficiently short for the signal to reach the voltage rail but too long for the signal to cross the voltage threshold during the first logic 1 following the string of 0s – resulting in an error: the 00001111 string would be identified as 10000111. A mixed example is shown in the bottom trace; here the 00001011 signal would be identified as 10000001.

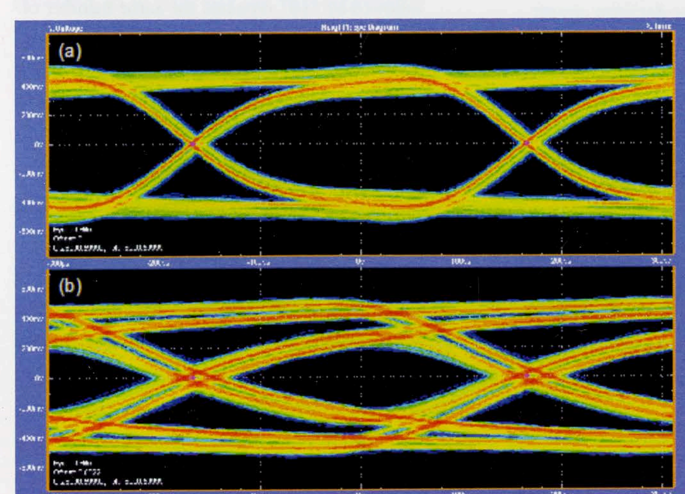

Figure 3 *Two signals on the same length of PCB, (a) at 3 Gb/s and (b) at 6 Gb/s.*

The ISI problem is compounded by impedance mismatches at connectors, which cause reflections, and unfortunate trace layout, which causes multipath interference. Further aggravating the situation, DCD and ISI do not combine in a linear way. This is one of the difficulties that face standards bodies as they attempt to define specifications that assure component interoperability.

The receiver – clock recovery, equalizer, decision circuit, and deserializer

At the receiver, a comparator first converts the differential signal, which then enters a complicated circuit. In Figure 1, the equalizer is portrayed to encompass the clock recovery and decision circuits because in most designs they're interrelated.

Clock Recovery

Recovering the clock at the receiver, whether or not the reference clock is distributed (dashed line in Figure 1) provides the opportunity to effectively filter the signal's low frequency jitter. The clock recovery circuit, whether based on a PLL or a Phase Interpolator (PI) and whether or not the reference clock is distributed, fabricates a data-rate clock signal based on the timing of the incoming waveform logic transitions. The resulting clock includes the low frequency jitter that is on the data. This way, when the recovered clock sets the timing of the decision circuit, the sampling point dances in rhythm with the lower frequency jitter. In other words: clock recovery serves as a high-pass jitter filter.

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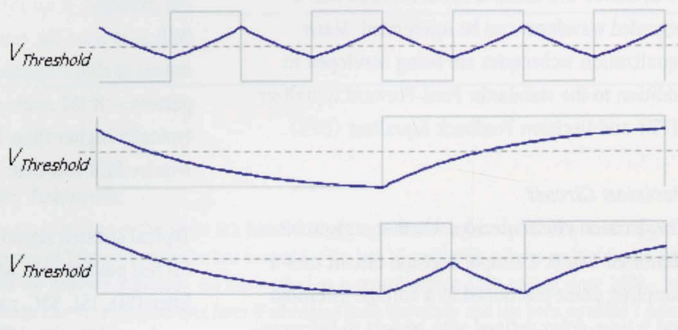
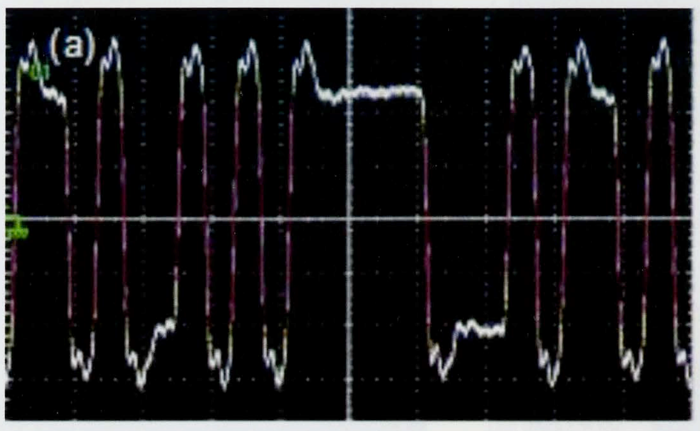


Figure 4 ***Simple examples of Inter-Symbol Interference (ISI). $V_{Threshold}$ is the logic-decision threshold, if the observed voltage is greater than $V_{Threshold}$ then the bit is identified as a 1, if less than $V_{Threshold}$, a 0.***

(...Continued) High-Speed Serial Signaling



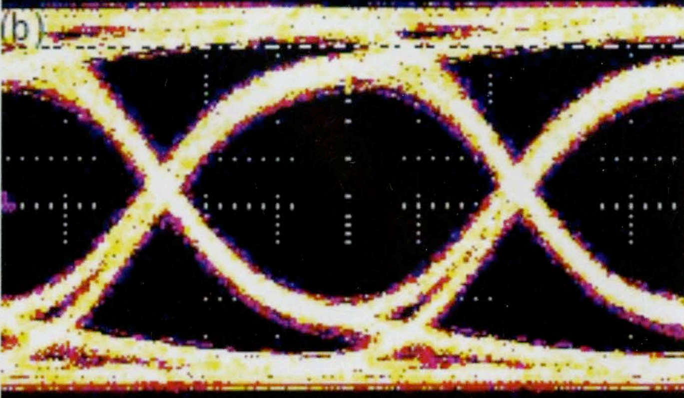


Figure 5 ***(a) De-emphasized signal at transmitter and (b) at receiver.***

The clock recovery circuit must have sufficient bandwidth for the recovered clock to track SSC. The clock recovery bandwidth is typically $f_{data}/1667$ – which should be ample.

De-Emphasis and Equalization

At ever higher data rates, ISI closes the eye. Since ISI is caused by the media and geometry of the transmission path, we can quantify the effect and account for it. At the transmitter, signal transitions can be *de-emphasized:* increasing the voltage magnitude of bits prior to transitions increases their high frequency content mitigating frequency response properties of the transmission path sufficient to open the eye at the receiver (Figure 5).

Receiver equalization involves a decision circuit that inverts the effects of the transmission path; we *equalize* the cause of eye-closure so that a degraded waveform can be interpreted. Many equalization techniques are being developed in addition to the standards: Feed-Forward Equalizer (FFE) and Decision Feedback Equalizer (DFE).

Decision Circuit

The decision circuit decides whether a given bit is identified 1 or 0. A simple decision circuit uses a sampling point positioned at a voltage threshold and a time-delay defined with respect to the recovered clock. If the voltage is larger than the threshold, V_{th}, at the time-delay, x_{sp}, it must be a 1, else it's a 0. Of course the (x_{sp}, V_{th}) position of sampling point is not an ideal point, both setup and hold times and voltage-slice sensitivity consume jitter and noise margin.

Stressed Receiver Tolerance Testing in Serial Data Systems

The receivers in serial data technologies have to be specified to assure their interoperability with transmitters, clocks, backplanes, cables, et cetera from different vendors. To assure that a receiver is adequate, it is tested under the most stressful conditions consistent with the technology specification. If the receiver can perform under the worst-case conditions at or better than the specified Bit Error Ratio (BER) then it's good to go.

Errors occur when logic transitions fluctuate across the sampling point of the decision circuit. For example, if an ISI trajectory causes an error, the BER is at least the ratio of the number of occurrences of that trajectory to the length of the stress pattern – if ISI alone causes errors the BER is typically higher than 10^{-4}. Most specifications require BER less than 10^{-12}.

Typical stressed signal transmitters generate a stressful test pattern with adjustable levels of Sinusoidal Jitter (SJ), ISI, SSC, random white noise and random white jitter (RJ), and an impairment that emulates crosstalk.

Test pattern effect on baseline wander

Serial data receivers are typically AC coupled. If the average voltage of a signal varies significantly, the baseline voltage wanders. AC coupling is stressed by varying the mark density of the signal. The mark density is the average fraction of logic ones in the data: the ratio of the number of logic ones to the total number of bits. Most standards require a mark density of ½; that is, equal numbers of ones and zeros averaged over the time scale of the system. The time scale is determined by the RC time constant of the receiver's AC coupling. Baseline wander is stressed by signals that vary from mark density of ½ over times shorter than, but close to, the specified RC constant. For example, a signal like 0010 repeated many times, followed by 1101 repeated the same number of times provides back-to-back AC coupling stress while satisfying the overall mark density = ½ requirement.

Test pattern effect on clock recovery

The clock recovery circuit functions by synthesizing a data-rate clock from the logic transitions of the input waveform. The more logic transitions, the easier it is for the receiver's clock recovery circuit. To this end, almost every standard requires that compliant signals have an average transition density of ½ – the transition density is the average number of logic transitions ($1 \rightarrow 0$ and $0 \rightarrow 1$) in a signal. A transition density of ½ means that, on average, half of the bits in the signal precede a transition. The most difficult signal to derive a clock from is a long string of Consecutive Identical (CID) bits – the fewer transitions, the less clock content in the signal. To stress the receiver, then, we put CID strings in the test pattern that challenge the clock recovery bandwidth.

Test pattern effect on inter-symbol interference

Inter-Symbol Interference (ISI) determines the average waveform, or "trajectory," of each bit in a signal. The trajectory is determined by the bit pattern immediately neighboring a given bit. The number of bits that affect the trajectory is given by the length of the pulse response. Thus, it is important to stress the receiver with every bit sequence that extends over the length of the pulse response – typically less than about eight bit periods.

Deterministic Jitter (DJ)

DJ can be separated into two categories: that which is correlated to the signal, like ISI, and that which is not, like Sinusoidal Jitter (SJ). As the name implies, SJ is sinusoidally varying phase modulation. ISI causes both jitter and voltage noise – eye closure in both the vertical and horizontal directions – and occurs at rational fractions of the data rate and with amplitudes that depend on the loss character of the transmission path.

Most standards require a combination of SJ and ISI, though some just require DJ and let the user choose the type. Emerging standards and, it is safe to expect, standards yet to come will not be so forgiving.

Random Jitter (RJ)

RJ is caused by the sum of many small effects like thermal oscillations in the clock, tiny variations in trace widths and conductor radii in cables and so forth. It is universally assumed to follow a Gaussian time domain distribution and to have a white frequency spectrum. The Gaussian assumption is the obvious statistical choice. The white frequency spectrum is a less obvious choice because the primary cause of random jitter, the oscillator driving the reference clock at the transmitter, tends to have a pink, flicker-dominated frequency spectrum.

The role of RJ in stressed receiver tolerance tests

RJ presents a small but important additional stress to the clock recovery circuit. It causes the timing of every DJ-defined edge to randomly fluctuate a small amount. Small random fluctuations stress the ability of the clock recovery circuit to remain steady and locked.

We can derive that the vast majority of RJ stresses are very small: over 99.7% of RJ occurrences are less than 10% of the peak-to-peak DJ. The vast majority of RJ effects are small amplitude fluctuations that occur with high probability.

Conclusion

A "receiver tolerance test" probes the ability of a receiver to work with a degraded input signal. The idea is to subject the receiver to a well defined worst case signal and require that it operate at a specified Bit Error Ratio (BER), usually 10^{-12} or lower.

We have reviewed receiver tolerance testing by emphasizing how each stress – the compliant pattern, rise/fall time, Sinusoidal Jitter (SJ), Inter-Symbol Interference (ISI), Random Jitter (RJ) and noise, and Spread Spectrum Clocking (SSC) – plays a unique role in testing the clock recovery, equalizer and decision circuit elements of receivers.

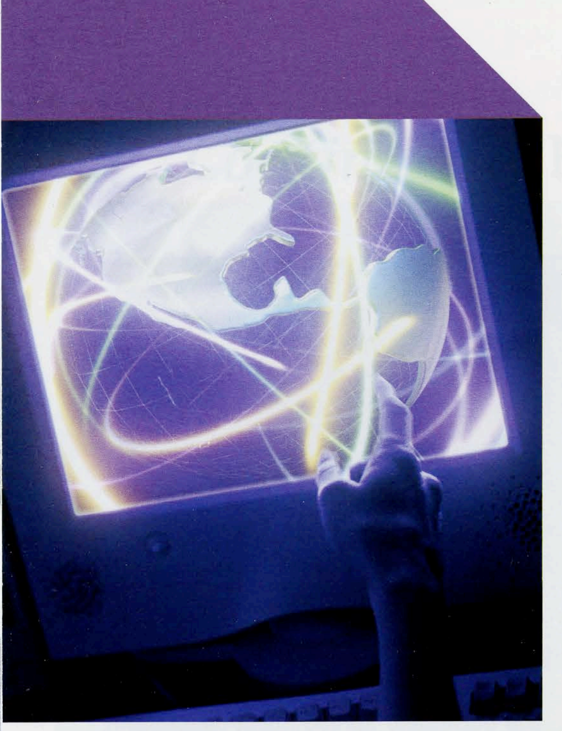
ABOUT THE AUTHORS

Ransom Stephens
Ransom's Notes

Ransom Stephens' company, Ransom's Notes, produces and presents content at every level of technical sophistication to help engineers advance to technology's cutting edge. He spent 13 years in basic-research laboratories and universities across the United States and Europe specializing in precise measurements of noisy signals. He is the author of over 200 articles in the electronics industry, science journals, and magazines, has introduced new measurement techniques for electrical and optical systems, invented methods for extracting signals from noise, led an engineering commando team, and served on high data-rate standards committees.

John Calvin
Principal Engineer, Tektronix

John Calvin currently is the chairman of the Serial ATA International Organization's Interoperability working group. John is a principal engineer at Tektronix where he has worked for the last 15 years with a focus on high speed serial measurements solutions for industry standards. He has worked as a contributor to SATA testing since 2000. John holds a Bachelors Degree in Electrical Engineering from Washington State University and has been awarded 7 patents in measurement-related technology.



Challenges — An Interview with Dr. Howard Johnson

I spent a full day getting here. First a flight to Seattle, then a puddle-jumper to a tiny town in rural, Eastern Washington State, and then a 90-minute drive high up into the Cascade Mountains have brought me to Signal Hill Ranch, the home of Dr. Howard Johnson, author of High-Speed Digital Design: A Handbook of Black Magic and many other publications (Figure 1).

No one knows what to expect when they arrive, do they?

Dr. Johnson replies, chuckling: No, they don't. When people pass the Idle-a-While motel on the highway they start wondering if they've made a wrong turn, but, when you finally get to the top of Signal Hill and fix your eyes on the gorgeous pastures, and see the horses, and drink in the incredible views, at that point the whole feeling of the place just melts your heart.

The feeling here in your office isn't bad, either. When did you move here?

My wife and I moved here in 1998 after a long search. Our oldest daughter was just entering 1st grade when we bought this old ranch. It took almost a full year to bring it up to livable condition.

It certainly looks nice now. I love the big logs and the snow-capped mountain views. It can't be easy to live this far from the city, though.

Your nearest neighbor is nearly a mile away. What motivated you to move way out here?

Moving here was not an easy decision. Living in the country is a difficult path, a challenging one that every day measures my resolve and my resourcefulness. That's what I like about it. The atmosphere here encourages one to look at problems in a different way, cutting to the real underlying causes of difficulties and finding new ways around them. It also breaks me out of what I call "urgent product development mode."

I spent years in Silicon Valley developing products—voicemail systems, robotics, serial transceivers, standards for Ethernet, all kinds of products. Here, I've assumed a new role researching issues, doing experimental work, and reporting results for the benefit of engineers around the world in the form of books, articles and movies.

How do you stay current?

I probably talk to as many engineers each year as anyone on the planet. My seminars and public presentations reach hundreds of individuals annually, plus many more than that write to me about their concerns. When I hear about some new part or tool, I call the manufacturer to check up on the details. That's enough to keep anyone up-to-date.

What concerns do your students face?

Three broad categories spring to mind. I don't mean that these are the only big challenges for digital designers, but, tools, probes, and materials seem to me three of the biggest problems we face. Progress in the areas of probes and materials seems very slow, just at a time when everyone is smacking up against their limitations. The laws of physics limit these subjects, so unless something dramatic happens I don't expect big solutions any time soon. The one bright spot is tools. CAD tools are made from software, which can and has dramatically improved over the past few years.

Specifics?

The integration of frequency-based and time-domain based toolsets strikes me as particularly important. We have had transmission line simulators for quite a while, but now we can incorporate lossy effects, S-parameter characterizations, and three-dimensional multi-port models into our signal integrity simulations. These elements are each reduced by the software to equivalent discrete circuits that execute in a SPICE-like manner with non-linear sources and loads.

Figure 1 **Signal Hill Ranch is nestled high in the Cascade Mountains on the sunny, rural Eastern side of Washington State.**

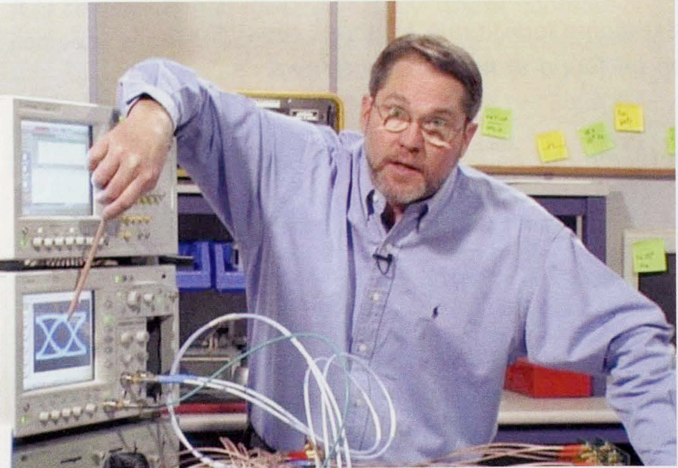


Figure 2 **Dr. Johnson researches issues, conducts experimental work, and reports results for the benefit of engineers all around the world.**

Even a few years ago, such processing was infeasible just due to the sheer magnitude of computation required. Today we find ourselves, to quote Newton, "standing on the shoulders of giants", the clear beneficiaries of generations of work speeding up computer hardware. All that prior work makes possible our advanced simulations, and that allow us to design even faster machines. It's a fantastic spiral of technological achievement.

How many digital designers use advanced simulation models today?

OK, here's the deal—very few. What we've got to do is convince these people that signal integrity simulation actually works and that it will definitely improve the robustness of their designs. Especially when you go above 1 Gb/s and further than 10 inches, simulation becomes indispensable.

What's special about 1 Gb/s and 10 inches?

The speed-distance limitation is what matters for pcb-scale products. For example, whether you work at 500 Mb/s going 20 inches, or 2 Gb/s at five inches you run into pretty much the same problems. High-frequency losses, reflections, and crosstalk can kill your circuit. Simulations help you see what you are doing.

Look at it this way. Nobody would drive next to the cliffs of Dover in a sports car with their eyes closed. It's obviously dangerous. One false move would plunge your car off the cliff.

The digital world imposes similar constraints. As you drive any design towards the ultimate limit of speed, or density, or line length, there comes a point where the performance falls off a cliff, so to speak. It fails, catastrophically. Bit errors, lost packets, whatever. Everything fails when sufficiently stressed.

The question is, how much stress can your design take before it goes bonkers, and how much stress do you have from natural variations in manufacturing plus the inevitable fluctuations in clock speed, power supply voltage, and temperature that come with real-world operation.

If your competitors use advanced tools to model their system performance then they can skirt closer to the edge of the cliff than you, without ever falling off. That means their products will go faster and further, with more channels, than yours. You cannot win that battle. You need to know precisely how close your circuit lies to the edge of malfunction and manage that spacing.

That is the purpose of signal integrity tools, and the reason I so much enjoy helping people understand how to use them.

So, you are hopeful about the future of high-speed digital design?

Yes, very much so. Digital engineers are a clever lot and have overcome many obstacles to get where we are today. No doubt that will continue.

Thanks for speaking with me today. This has been a most interesting trip.

I am glad you were able to make it. Thanks for coming all this way to visit. I hope you won't be running back to the office first thing?

Well, maybe next time I can schedule a little more time to enjoy the view while I'm here…

Figure 3 **The atmosphere at Signal Hill Ranch encourages one to look at problems in a relaxed way.**

ABOUT THE INTERVIEWEE

Howard Johnson

Howard Johnson, PhD, author of High-Speed Digital Design and High-Speed Signal Propagation, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. www.sigcon.com, howie03@sigcon.com.

HKN Award Nominations

*HKN invites its members to nominate outstanding individuals for these prestigious awards. Nomination details and forms can be found at **www.hkn.org/awards**.*

Outstanding Young Electrical and Computer Engineer

- *Presented annually to an exceptional young engineer who has demonstrated significant contributions early in his or her professional career*
- *Nominations due April 1*

Vladimir Karapetoff Outstanding Technical Achievement Award

- *Recognizes an individual who has distinguished himself or herself through an invention, development, or discovery in the field of electrical or computer technology*
- *Nominations ongoing*

Distinguished Service Award

- *Acknowledges an individual who has devoted time and energy to the Eta Kappa Nu Association through years of active participation*
- *Nominations ongoing*

Outstanding ECE Student Award

- *Annually identifies an ECE senior who has proven outstanding scholastic excellence; high moral character; and exemplary service to classmates, university, community, and country*
- *Nominations due June 30 to the LA Alumni chapter*

Outstanding Chapter Award

- *Singles out chapters that have shown excellence in their activities and service at the department, university, and community levels*
- *Winners are determined by their required Annual Chapter Reports, due October 15 for the preceding academic year*

C. Holmes MacDonald Outstanding Teaching Award

- *Presented annually to a dedicated young professor who has proven exceptional dedication to ECE education and has found the balance between pressure for research and publications and enthusiasm and creativity in the classroom*
- *Nominations due November 1*

Notes from Headquarters

Dear HKN Chapters, Here are a few friendly reminders from the HQ office:

- **HKN HQ moved!** Please download new forms from www.hkn.org and update your contact records as appropriate.

HKN Headquarters
445 Hoes Lane
Piscataway, NJ 08854 USA

Phone: 1-800-406-2590 • Fax: 1-800-864-2051
Email: info@hkn.org • Web: **www.hkn.org**

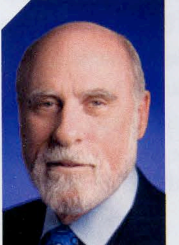
- Don't forget to send your New Member Requisition Form and dues for your inductions to HQ. Inductees are not considered HKN members until all of the paperwork has been processed. If you have not received the certificates, HQ has not received the paperwork.
- If you are an IEEE member, please let us know what your IEEE member number is and the School, Chapter, and Year in which you were inducted so that we can code your records appropriately. Send a message to HKN Headquarters at **ieee-hkn@ieee.org**.
- Looking for career services? Registration is free for Experience, Inc. **www.hkn.experience.com** Log in to upload your resume, search for jobs or connect with other HKN members. Another free networking group is available on LinkedIn. **www.linkedin.com**
- Nominate an outstanding colleague for an HKN Award! All nomination forms are available online as well as the deadlines for submission.

*As always, the HKN Web site **(www.hkn.org)** is the best source of information, paperwork, project ideas, award information, and upcoming activities.*

Two New Eminent Members Inducted

Eta Kappa Nu established the rank of Eminent Member in 1950 as the society's highest membership classification. It is conferred upon those select few whose contributions and attainments in the field of electrical and computer engineering have resulted in significant benefits to humankind.

EMINENT MEMBER — Presented June 2010



Vinton G. Cerf

Cerf earned his title as one of the "Fathers of the Internet" for his work as co-designer with Robert Kahn of the TCP/IP protocols and the architecture of the Internet. During his tenure from 1976-1982 with the U.S. Department of Defense's Advanced Research Projects Agency (DARPA), he played a key role leading the development of Internet and Internet-related packet data and security technologies. In addition to his work on behalf of Google and the Internet, Cerf has served as a technical advisor to production for "Gene Roddenberry's Earth: Final Conflict" and made a special guest appearance on the program in May 1998. Cerf has appeared on television programs NextWave with Leonard Nimoy and often co-hosted World Business Review with Alexander Haig and Caspar Weinberger. Cerf also holds an appointment as distinguished visiting scientist at the Jet Propulsion Laboratory where he is working on the design of an interplanetary Internet.

Cerf at a Glance

- Vice President and Chief Internet Evangelist, Google
- Senior Vice President of Technology Strategy, MCI
- Vice President, Corporation for National Research Initiatives
- National Medal of Technology, ACM Alan M. Turing Award, Presidential Medal of Freedom, Japan Prize
- B.S. in mathematics from Stanford University; M.S., Ph.D. in computer science from University of California, Los Angeles

EMINENT MEMBER — Presented May 2010

Abraham Lempel

Widely known for his pioneering work in data compression, Lempel is co-inventor of the Lempel-Ziv (LZ) data-compression algorithm, a universal noiseless source-coding technique. In addition to his personal contributions as a researcher, he has helped to foster the careers of others as an academic leader at Technion, where he has served on the faculty for more than three decades, and as founder of HP's Israel lab, which focuses on color printing algorithms, compression and coding algorithms, image processing and computer vision algorithms and document processing and understanding. Lempel's association with HP Labs began in 1984 when he visited the Palo Alto headquarters during a sabbatical. In 1994, with the establishment of HP Labs Israel, he became a full-time HP employee, on special leave from Technion, where he is still a chaired professor of Computer Science, holding the Viterbi Chair in Information Systems.

Lempel at a Glance

- Emeritus Professor, Technion – Israel Institute of Technology
- HP Senior Fellow, Hewlett-Packard
- Director, HP Labs Israel, HP Labs Advanced Studies Program
- Dean, Computer Science, Technion – Israel Institute of Technology
- IEEE Fellow, IEEE Information Theory Society Golden Jubilee Award, ACM Paris Kanellakis Theory and Practice Award, IEEE Milestone in Electrical Engineering and Computing, IEEE Richard Hamming Medal, Rothschild Prize in Engineering
- B.Sc., M.Sc., and D.Sc. in electrical engineering from Technion – Israel Institute of Technology

Member Profiles

Adam Cron
Principal Engineer
Synopsys
Member, Gamma Eta

Career Highlights

Texas Instruments fostered individual responsibility. One of my favorite projects there was designing a set of chips and boards to demonstrate a new test architecture. I was given a lot of responsibility; worked long, satisfying hours; and finished in time to show the fruits of our labors at the most important test industry conference. I was also lucky to work at several "start-ups" at Motorola. I was responsible for designing, subcontracting, and programming test systems to filter good products from bad. Heavy responsibility resulted in much gratification when the first products passed testing and were heading to places like Best Buy and Dell Computer.

Education and Career

To be challenged in college, and rise up to that challenge is more important than one might think. First, it proves to an employer that you have some smarts and can learn new things when you have to. Second, it prepares you for situations which, frankly, you hope to encounter on the job: challenging tasks and responsibilities that fall squarely on your shoulders.

Advice to Engineering Graduates

Matching a particular set of classes with a particular job is probably more luck than planning. Go for what you love and hope it pans out into a job you enjoy. Choose a varied curriculum: it is better to be flexible and adaptable than singularly focused. Also, don't be frustrated by not landing the job of your dreams on the first try. The job you "want" you might hate, and the job you get you might love. Embrace the adventure.

David Horowitz
Consultant and Principal
Horowitz Television Technology
Member, Beta Alpha

Career Highlights

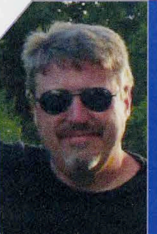
At CBS, I rose from a design engineer in audio/video engineering in 1965 to the Vice President of Planning before I left in 1990. I established my own consulting company, Horowitz Television Technology, which has been very successful over the last 20 years serving many great clients such as PBS.

Education and Career

My education at Central High School in Philadelphia prepared me so well for Drexel with the result that I started to coast. Midway through my BS I had to re-apply myself but did graduate on time. Computer switching theory and logic courses turned out to be very useful in systems design work. Humanities courses are essential in rounding out one's education preparing you for interaction with real people in your job and social life.

Advice to Engineering Graduates

Keep your eyes and ears open, your mouth closed until you are asked your opinion. Read the "Unwritten Rules of Engineering" originally published in 1944 by W.J. King but an updated version is available with a simple Internet search. Also read the 1899 "Message to Garcia" written by Elbert Hubbard. It is all about taking the initiative.



Mark A. Jay
Proprietor, Principal Engineer
Immersifi Recording Technologies
Manager, Noise, Vibration, Harshness & Sound Quality
Lear Corporation
Member, Iota Epsilon

Career Highlights

I have been exposed to some wonderful things in my professional career. I have been able to design and invent things, and mentor co-op students and entry-level engineers. I have been able to write technical papers with some very clever people, learning from them and growing in the process. My day-job is very focused on the objective and subjective sides of sound, but my own company is highly focused on the aesthetics of sound.

Education and Career

Without a doubt, being trained as an engineer made my career possible. All engineering degrees have at their core the same thing: giving the student a structured approach to problem-solving. I always had an interest in sound and acoustics, but I chose to pursue electrical engineering because I felt that I needed to make my thinking more structured. All of my years in the automotive sector allowed me to learn about acoustics, sound, human perception, signal processing, statistics, etc., but they also opened doors – and my mind – to the possibility of starting my own recording business, specializing in binaural recording.

Advice to Engineering Graduates

Follow your technical and life passions, but always keep an eye open for opportunities that, at first, may seem un-related or tangential to your desired specialty. I personally envisioned myself working in the field of amplifier design. However, the path I have chosen, or better, had given to me, has been an extremely rewarding and challenging one.

Eta Kappa Nu Association Financial Report

For the year ended June 30, 2010 (Reviewed)

STATEMENT OF FINANCIAL POSITION

ASSETS	
CURRENT ASSETS	
Cash and cash equivalents	$163,601
Membership and contribution receivables	10,896
Awards inventory	8,869
Prepaid expenses	276
Total current assets	183,642
INVESTMENTS – at Market Value	338,628
Total assets	$522,270

LIABILITIES AND NET WORTH	
CURRENT LIABILITIES	
Accounts payable	$5,208
Total current liabilities	5,208
LONG TERM LIABILITIES	
Unearned subscription revenue	404,033
NET ASSETS	
Unrestricted	113,029
Total liabilities & net worth	$522,270

STATEMENT OF ACTIVITIES

REVENUE	
Memberships	$99,071
BRIDGE magazine subscription	17,465
Merchandise sales (net of $6,717 of costs incurred)	11,088
Contributions	7,074
Sponsorships	5,308
Total Revenue from Operations	140,006
OPERATING AND ADMINISTRATIVE EXPENSES	
Management fee	126,282
Awards	12,418
BRIDGE production	34,331
Chapter support	15,829
Directors, officers and committees expense	21,847
Office and administrative expenses	7,567
Professional fees	8,573
Total Operating and Administrative Expenses	226,847
Net loss from operations	(86,841)

OTHER INCOME (EXPENSES)	
Dividends and Interest	$9,776
Realized loss on the sale of investments	(13,104)
Market value appreciation of investments	95,136
Investment advisory fees	(4,933)
Net Other Income	86,975
NET SURPLUS	34
NET ASSETS – BEGINNING OF YEAR	112,995
NET ASSETS – END OF YEAR	$113,029

STATEMENT OF CASH FLOWS

CASH FLOWS FROM (USED FOR) OPERATING ACTIVITIES	
Cash received from memberships, contributions and program activities	$127,394
Cash paid for operations	(282,623)
Net cash used for operating activities	(155,229)
CASH FLOWS FROM (USED FOR) INVESTING ACTIVITIES	
Investment earnings – net of advisory fees	4,843
Proceeds from the sales of investments	202,586
Purchase of marketable securities	(10,610)
Net cash from investment activities	196,819
NET INCREASE IN CASH AND CASH EQUIVALENTS	41,590
CASH AND CASH EQUIVALENTS BEGINNING OF YEAR	122,011
CASH AND CASH EQUIVALENTS END OF YEAR	$163,601

Reconciliation of Net Gain to Net Cash Used for Operating Activities

NET SURPLUS	34
ADJUSTMENT TO RECONCILE NET GAIN TO NET CASH USED FOR OPERATING ACTIVITIES	
Investment activity attributable to investing activities	(86,875)
Cash received or expended to	
Increase in accounts receivables	(7,791)
Decrease in inventories and prepaid expenses	1,428
Decrease in accounts payable and accrued expenses	(50,487)
Decrease in unearned subscription revenue	(11,538)
Net cash used for operating activities	($155,229)

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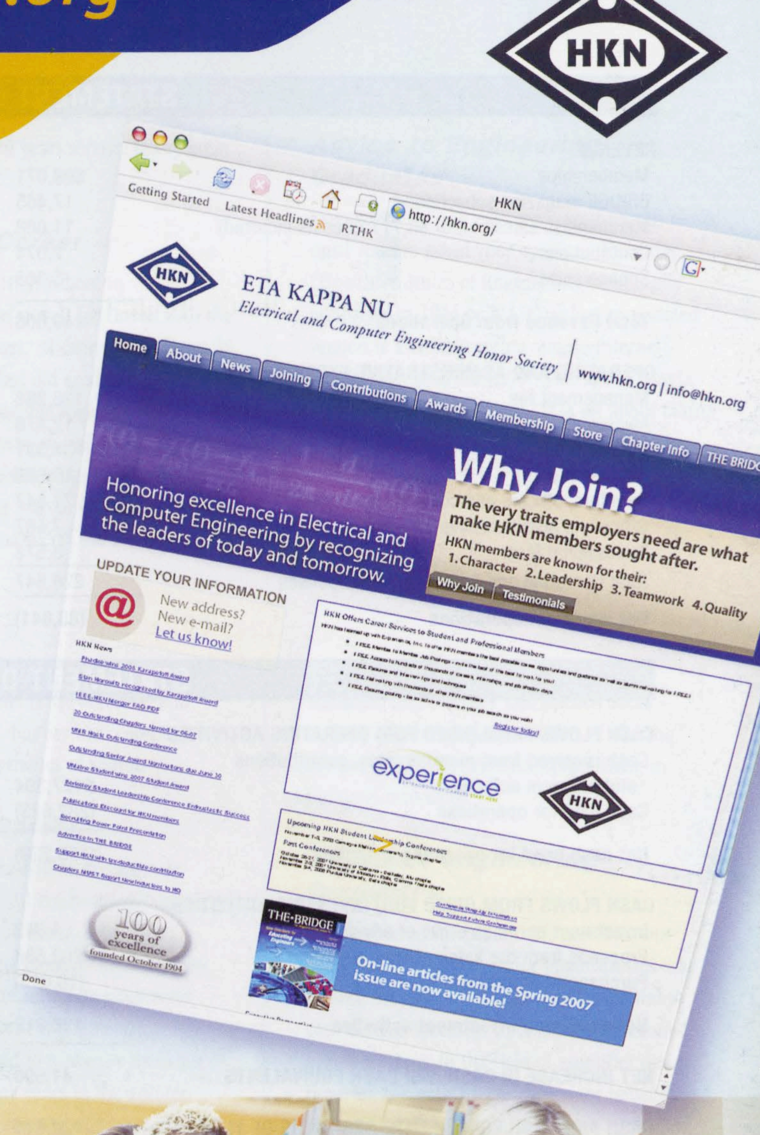

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