84 T&D 385-1

ADVANCED SCHEME FOR AC VOLTAGE CONTROL AT HVDC CONVERTER TERMINALS

A. Hammad
Senior Member IEEE

K. Sadek
Non Member

H. Koelsch
Non Member

G. Gueth
Member IEEE

BBC, Brown Boveri and Co. Ltd.
5401 Baden, Switzerland

Abstract:

A new economic and effective scheme for controlling the ac voltage at the HVDC terminals during both steady state and dynamic conditions is presented. By extending the basic characteristics of an HVDC converter, it is possible to affect and modulate the reactive power balance on the ac side. Analytical studies as well as digital and simulator results are presented to demonstrate the viability of the proposed ac voltage control strategy to optimize HVDC terminal design and performance for a practical system. The economic and technical features of the new scheme are discussed and compared with other ac voltage control techniques such as synchrononous condensers and static VAr compensators.

INTRODUCTION

HVDC converters of dc transmission or back-to-back schemes require reactive power at their commutating ac bus for their operation. Due to the delay angles associated with commutation overlap and dc current or dc voltage controllers and to avoid commutation failures, the ac fundamental current at an HVDC terminal always lags the ac commutating voltage. Whether in rectifier or inverter mode of operation, dc converter terminals absorb reactive power in proportion to their real power conversion. For conventional HVDC schemes, this proportion is approximately 60% during steady state conditions. If the host ac system has a relatively high source impedance, it cannot supply this reactive power without the ac bus voltage falling to an unacceptable low level. To avoid this, compensating shunt capacitor banks are oftentimes applied at the ac bus of the HVDC terminal. Some of these banks also serve as harmonic filters to short circuit the harmonic currents generated by the converters. However, a sudden disturbance in the reactive power balance at the ac/dc interconnecting point would cause , in this case, high fundamental frequency overvoltages[1]. These overvoltages are usually an essential factor in the design of most of the HVDC converter components and its associated ac apparatus.

To include such high overvoltages in the design of the dc converter terminal is quite costly, apart from the fact that they will be transmitted to other parts of the network along the ac transmission and distribution systems. Furthermore, all the equipment will be subjected to high voltage stresses which can often exceed their design value. Thus a prime objective would be to limit such overvoltages in an economic and effective manner. This calls for fast corrective measures to regulate the net reactive power exchanged with the ac system at the dc converter terminal and maintain its ac voltage within permissible limits[2,3]. The HVDC converter design can then be optimized in terms of cost and overall system performance. For this purpose, synchronous condensers and static VAr compensators have been considered. However, they constitute an additional equipment that has to be added to the total cost of the HVDC converter terminal.

This paper develops a new economic ac voltage control technique utilizing the HVDC converters themselves to effectively control the ac voltage during steady state conditions and to limit its transient excursions following ac or dc system disturbances. By extending the basic characteristics of an HVDC converter, it is possible to affect and modulate the reactive power balance at the interconnecting ac bus[4-7]. To achieve such a feature in a HVDC scheme, few additions and modifications are required in the operation and controls of HVDC converters. Such modifications are incorporated in an advanced control scheme that can be utilized for back-to-back and for long distance HVDC applications. By this method, the HVDC terminals can be made self sufficient in terms of ac voltage control, thereby making HVDC schemes more economically attractive.

Problems of ac voltage regulation and instability at an HVDC terminal are first quantified analytically by means of a simplified mathematical model. The effectiveness of the developed voltage control technique is then examined. To prove the viability of the proposed control strategy, digital simulations of system fundamental frequency as well as HVDC simulator studies are presented for the complete ac/dc systems for practical cases. The economic and technical features of the new control scheme are also demonstrated in comparison to synchronous condensers and static VAr compensators.

PROBLEMS OF AC VOLTAGE STABILITY AT HVDC TERMINALS

Large ac voltage fluctuations are considered to be a persistent problem associated with HVDC schemes when connected to relatively weak ac systems. To estimate the extent of those voltage variations, the criterion of short circuit ratio (SCR = short circuit capacity of the ac system at the HVDC converter side/nominal dc power) has been consistently used. However, such a simplistic approach does not take into consideration the voltage/reactive power characteristics of the ac network nor the operating control mode of the HVDC scheme. It is also not suitable for including the effects of static means for voltage support. Therefore, it is essential to define a more adequate criterion for ac voltage sensitivity in which the effects of HVDC operating and control modes, ac system damping as well as reactive power compensation methods can be taken into account.[8]

Voltage Stability Criterion

To derive the voltage stability criterion and to fully examine the influence of various system parameters and operating conditions, an appropriate simplified mathematical model is developed.

84 T&D 385-1 A paper recommended and approved by the IEEE Transmission and Distribution Committee of the IEEE Power Engineering Society for presentation at the IEEE/PES 1984 Transmission and Distribution Conference, Kansas City, Missouri, April 29 - May 4, 1984. Manuscript submitted November 4, 1983; made available for printing March 28, 1984.

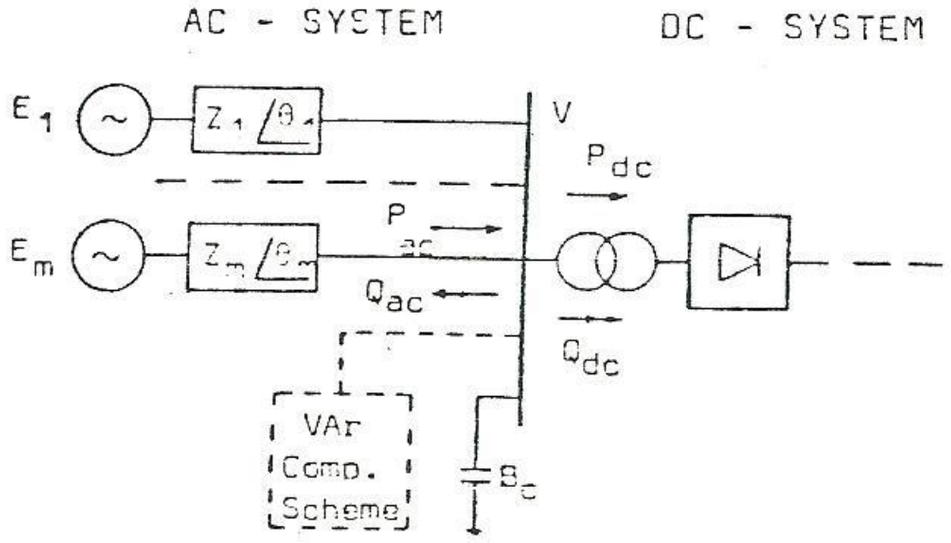

Fig. 1 Simplified system model for ac/dc interconnection point

The model representing the ac/dc interconnection point is as shown in Fig. 1. The ac system is represented by constant voltage sources behind fixed impedances, i.e. constant impedance loads. The total reactive power demand of all ac lines terminated at the interconnection point to maintain a constant voltage V at the HVDC terminal is Qac. For the case studied, where the short circuit ratio SCR at the dc rectifier terminal is 2.4, the variation of Qac as a function of dc power transmitted is as shown in Fig. 2. Both Qac and Pdc are expressed in per-unit basd on nominal dc power Pdn.

The HVDC converter is modeled by its linearized system of equations where small variations of dc current, dc voltage and firing (or extinction) angle are allowed. Fixed converter transformer taps are assumed at each operating point. Initial reactive power compensation at the HVDC terminal is assumed to be carried out by means of filters and capacitor banks. These can be represented in the fundamental system frequency as a lumped shunt capacitive sucseptance Bc.

As a measure of ac voltage stability, the "Voltage Stability Factor" VSF is defined at a specific dc power level Pdo as:

$$VSF = \Delta V/\Delta Bc \Big|_{Pd = Pdo} \qquad (1)$$

where ΔV is the incremental voltage change due to a small change in the shunt capacitance ΔBc.

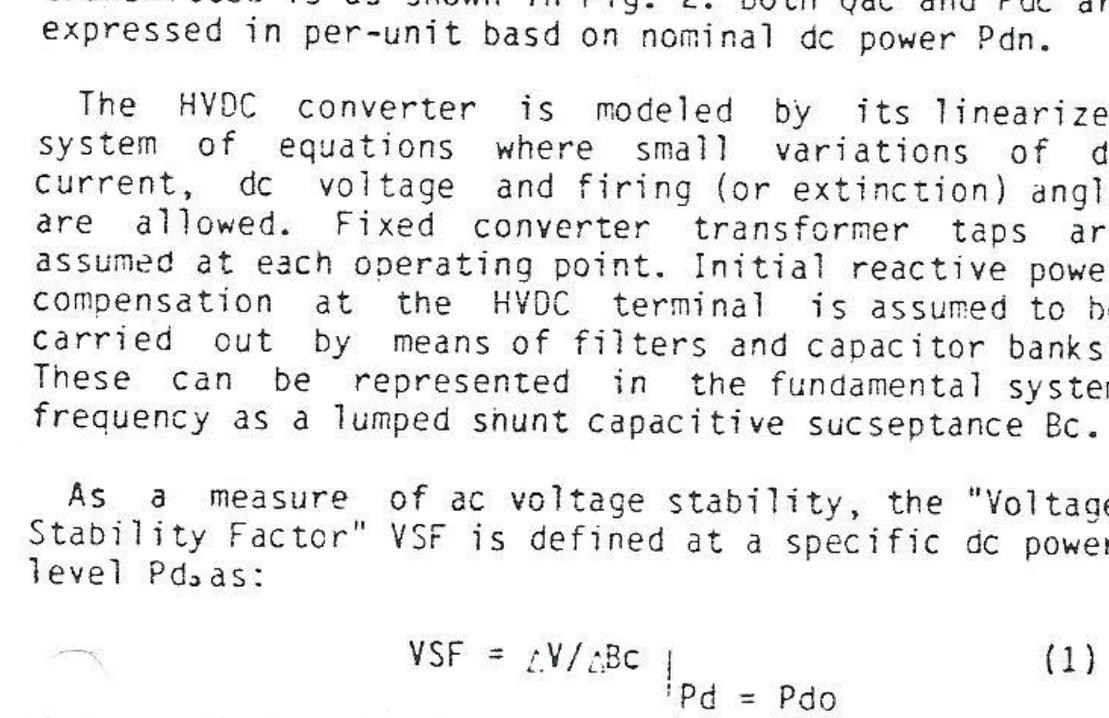

Fig. 2 Total reactive power demand of ac network at HVDC converter terminal

Fig. 3 shows the plots of "VSF" under different operating conditions. Curve (a) represents a weak ac system with SCR=2.4 and no VAr compensation. The dc converter is operating with conventional constant firing (or extinction) angle mode. Instability occurs in the vicinity of 0.8 pu dc power level and above. In this region large excursions of ac voltage can arise on account of any small variation in Bc. Curve (b) corresponds to a strong ac system with SCR=3.5 and the same Qac/Pdc characteristics of Fig. 2.

When the dc converter is operating with constant dc current, similar ac voltage instability characteristics are produced.

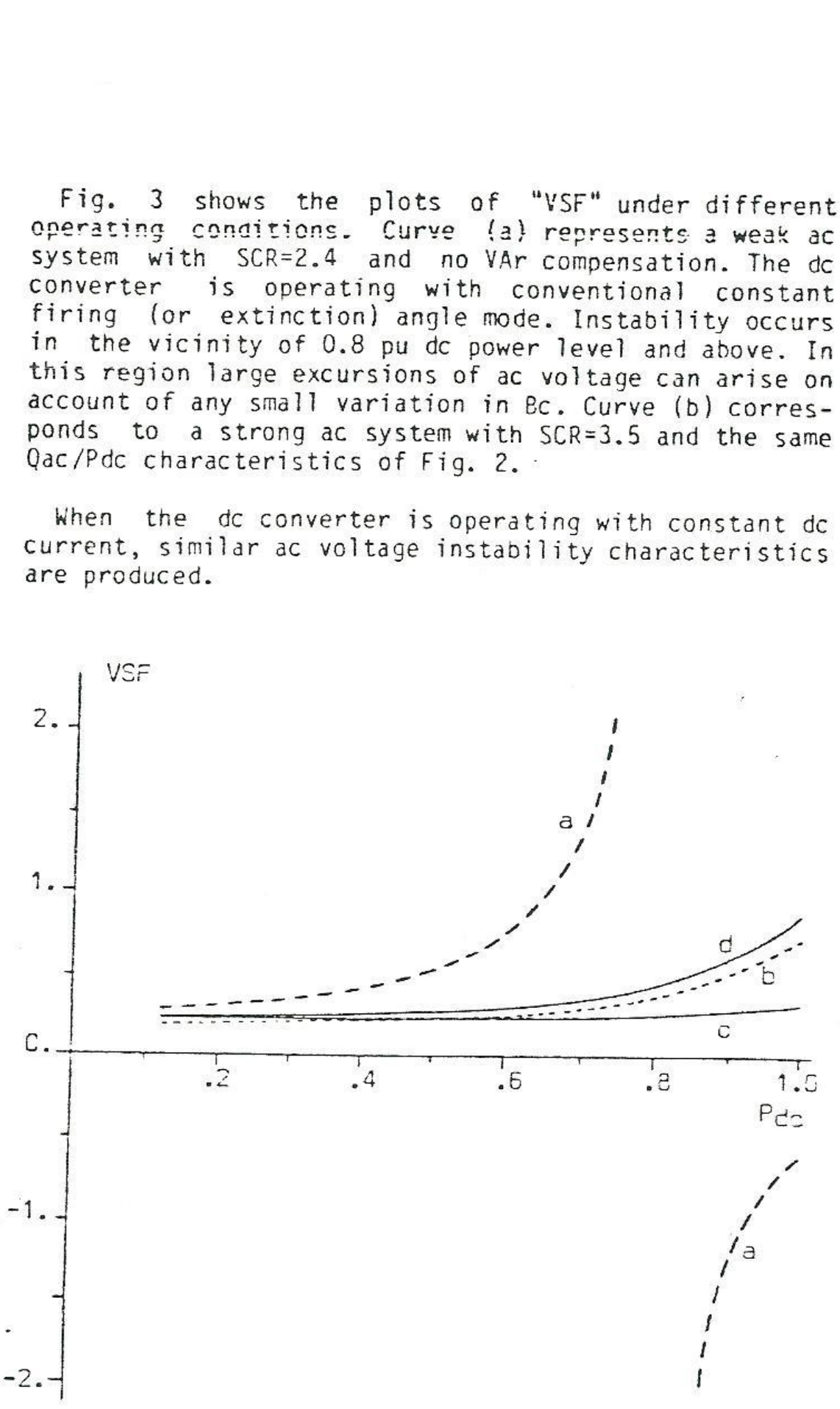

Fig. 3 Voltage Stability Factor at the HVDC terminal
(a) with no VAr compensation (SCR=2.4)
(b) for a stiff ac system - with synchronous condensers (SCR=3.5)
(c) with static VAr compensators (SCR=2.4)
(d) with HVDC converter controls (SCR=2.4)

Two major reasons can be thought of to be behind such a phenomenon: a) complete VAr compensation for a relatively weak ac system is attempted by means of static shunt elements (filters & capacitors) ; b) the HVDC converter operates with almost the same firing (or extinction) angle near its minimum value. In this case, the incremental change of reactive power absorbed by the dc terminal to the change of ac voltage ($\Delta Qd/\Delta V$) is always negative as depicted by curve (a) in Fig. 4.

AC Voltage Stabilization

Keeping in mind the very reasons for ac voltage instability at the HVDC terminals, we can logically arrive to the effective solutions for this problem.

The obvious and classical solution would be to increase the short circuit level at the ac/dc interconnection point. Synchronous condensers have been used in the past for such a purpose. However, they proved to be uneconomical, have high losses, and suffer from slow response compared to other static techniques. They can also deteriorate the overall ac/dc performance due to

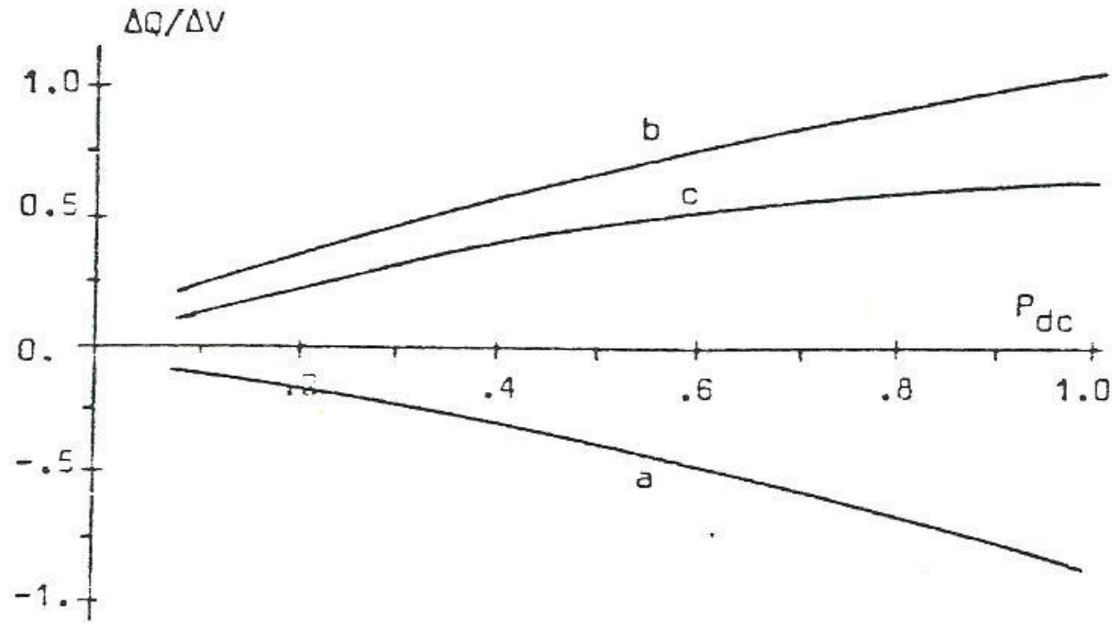

Fig. 4 Linearized ac/dc system (ΔQd/ΔV) performance
(a) with no VAr compensation
(b) with static VAr compensators (ΔQd+ΔQs)/ΔV
(c) with HVDC converter controls

their inertial oscillations following system disturbances. The voltage stability factor VSF for this case will be similar to that shown in Fig. 3 (b).

As a second alternative, regulated reactive power compensation can be achieved by means of static VAr compensators (SVC), such as thyristor controlled reactors, thyristor switched capacitors, or a combination of both. In this case the incremental change of reactive power of the SVC to the ac voltage change (ΔQs/ΔV) can be made to be positive in the complete range of Pdc. The combined SVC and HVDC converter reactive power to voltage incremental change (ΔQs+ΔQd)/ΔV is as shown in Fig. 4(b). Since the SVC are assumed to have the appropriate rating (0.35 pu) to fully control the ac voltage under all steady state loading and transient conditions, the instability problem is eliminated as shown by the VSF in Fig. 3 (curve c).

A third, and most reliable and economic solution, is to regulate the reactive power consumed by the dc converter Qdc in response to ac voltage variations. This can be realized by a localized ac voltage regulator acting directly on the converter firing controller. As the ac voltage increases, for example, a high firing angle order in case of rectifier (or extinction angle in case of inverter) is produced by the voltage regulator and overrides the signals from other regulators. Thereby, Qdc increases to limit the overvoltage.

In other words, the HVDC converter is made to act in a manner similar to a thyristor controlled reactor SVC type without impairing its basic converter characteristics. By this technique, the ratio ΔQd/ΔV is positive as shown in Fig. 4(c). Voltage instability is considerably reduced and the VSF is as shown inFig. 3(d).

It is interesting to note that under this operating mode with SCR = 2.4 the overall system has a stabilized performance almost identical to the stiff system with SCR = 3.5 . Therefore, temporary overvoltages expected in this case with the weak ac system would be in the same level as those for the stiff system. This will be demonstrated in the next sections.

This example clearly shows that even though the SCR can still give an indication of the overall properties of the combined ac/dc system, it fails to describe the exact ac voltage behavior under different VAr compensating conditions. In fact, if the Qac/V or Qac/Pdc demand characteristics are changed, different voltage stability characteristics would be obtained for the same SCR.

PRINCIPLES OF PROPOSED CONTROL TECHNIQUE

In order to establish the overall control strategy to simultaneously limit temporary overvoltages and enhance the performance of the dc system during and after fault conditions, the principles of ac voltage control method by the HVDC converter are first focused. A simple case is examined where the control action made by the HVDC converter (whether in rectifier or inverter operation) can be explained. For this purpose, a complete dynamic non-linear model for the full ac/dc systems is used for simulating the exact time response of the overall system. The digital simulations (shown in Fig. 5) have been performed by means of the BBC Power System Simulation Programs[3] where comprehensive fundamental frequency system models are utilized.

For simulating the disturbance, a capacitor bank (0.175 pu) is assumed to be switched on while the HVDC is operating at 100% load. This excessive amount of reactive power at the interconnecting bus can be effectively compensated by the reactive power absorption of the HVDC converter if the latter is properly controlled for this purpose. As shown in Fig. 5, a temporary overvoltage is produced with a peak of 11%. However,by advancing the firing angle α , the dc voltage is reduced and the Qdc absorbed by the dc converter is increased. The ac voltage is quickly controlled back to 1.0 pu.

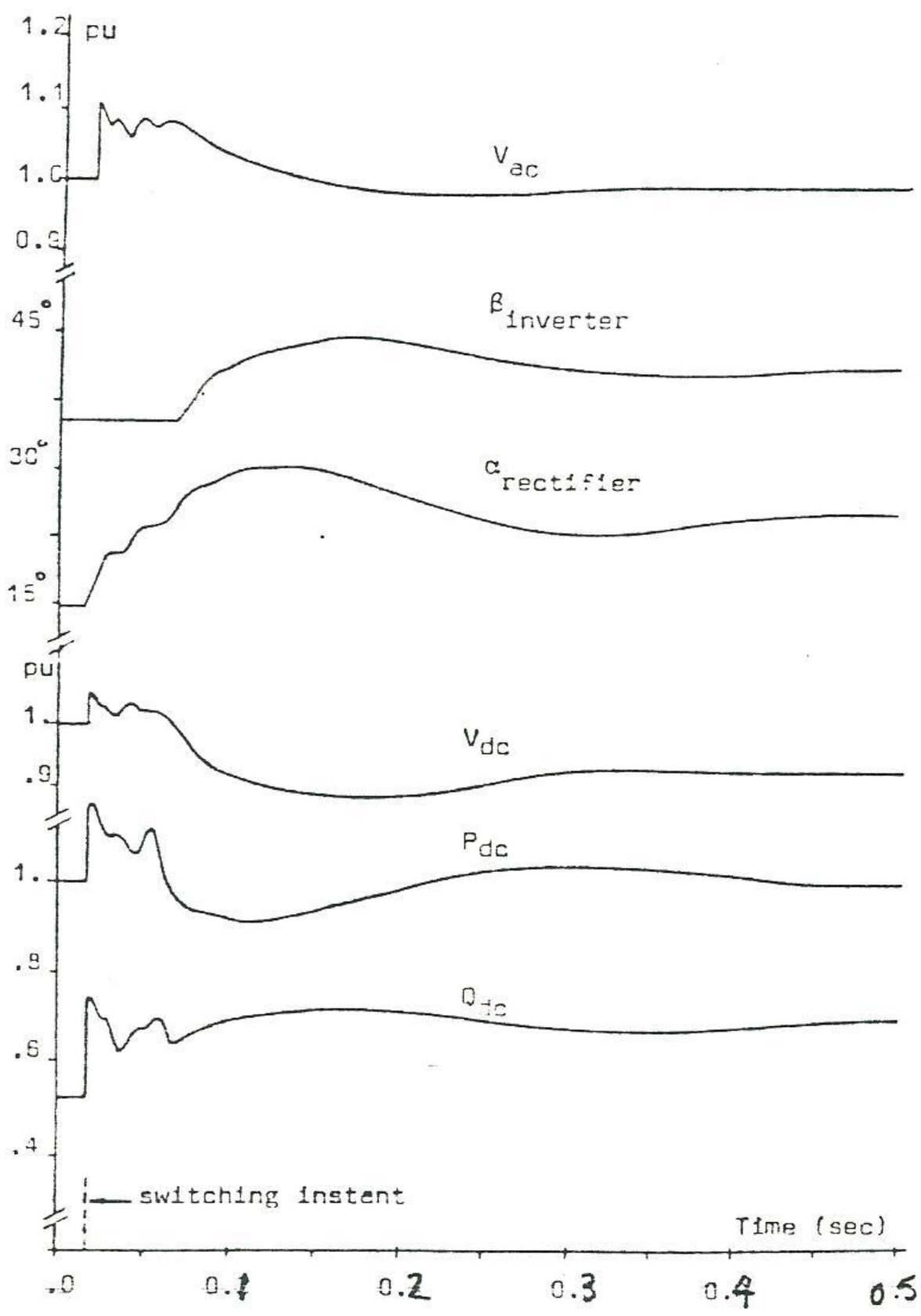

Fig. 5 Digital simulation for switching on a 0.175 pu capacitor bank at the dc terminal with ac voltage control mode of HVDC converters

The same system has been modeled in the BBC HVDC simulator but with the full representation of filter banks and ac system sequence impedances and saturtion effects and employing a scaled thyristor valves and actual controllers.[10] The transient behavior of the 3-phase ac voltage during switching 'on' the reactive power unit with the voltage controller in operation is as shown by the traces of Fig. 6.

The evident match between the results obtained by digital and analogue simulations in Figs. 5 and 6 respectively, clearly demonstrates the viability and effectiveness of the proposed technique.

Description of Basic Controls

It is common practice to use an HVDC converter terminal to help stabilize the interconnected ac system. Primarily, this is achieved by modulating the dc power, through the dc power order, in accordance with the ac system frequency variations. The oscillations or modulations , known as "inertial oscillations", are characterized by slow frequency (1~2 Hz). In principle, a similar action can be exerted but to affect the HVDC reactive power absorption and consequently controlling the ac voltage adjacent to the dc terminal. This control mode, however, is characterized by the relatively fast voltage oscillations compared to the system frequency (inertial) oscillations. Under this condition an HVDC converter can be looked upon as a static VAr compensator with a rating ultimately equals the full MVA rating of its converter transformer. That is because a dc converter absorbs reactive power according to:

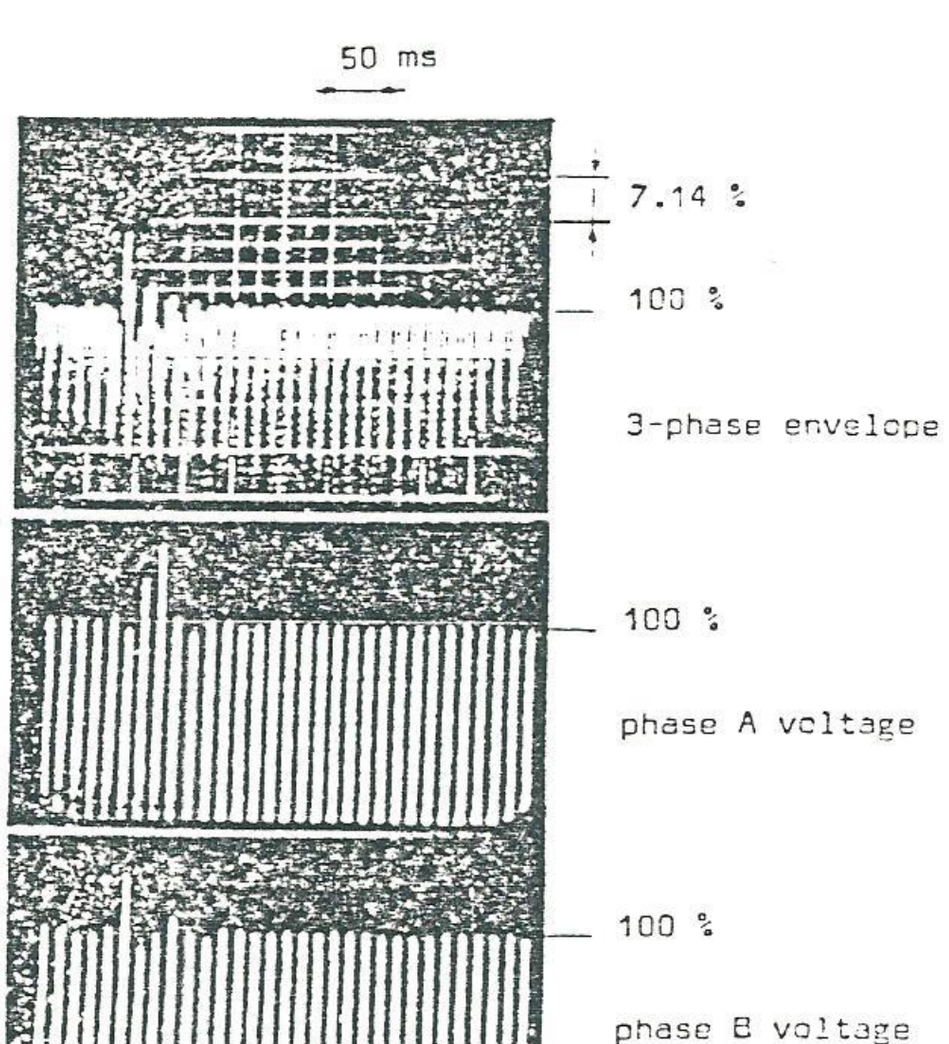

Fig. 6 Transient 3-phase voltages for switching on a 0.175 pu capacitor bank at the dc terminal with HVDC converter controls

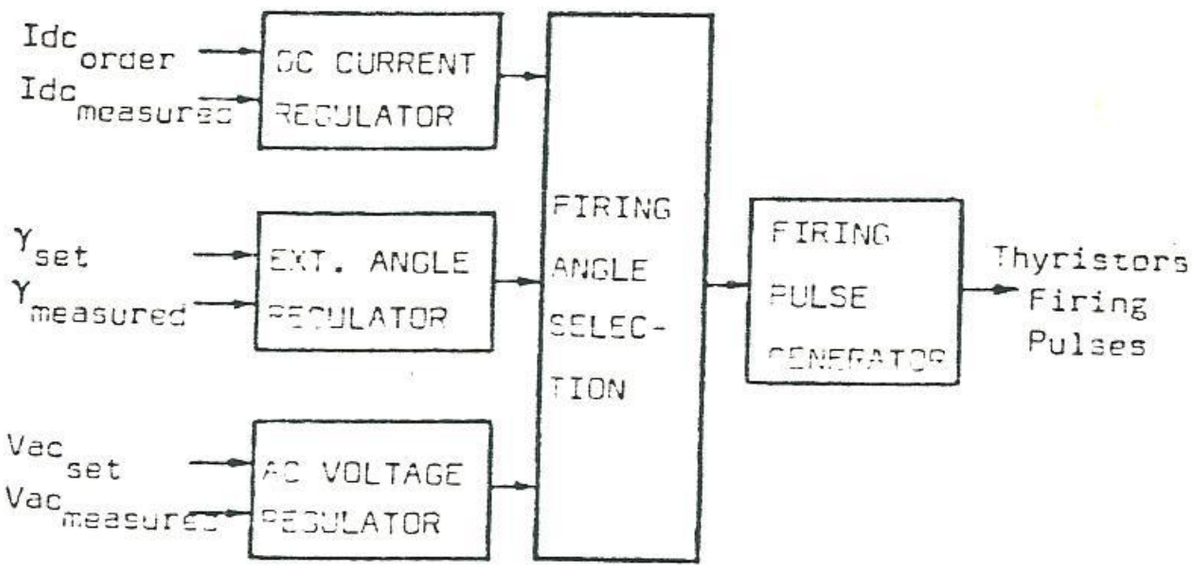

Fig. 7 Simplified diagram for proposed control scheme of a HVDC converter

$$Qdc = Vdc \cdot Idc \cdot \tan \phi \quad (2)$$

where

$$\cos \phi = Vdc(pu) / Vac(pu) \quad (3)$$

and

$$Vdc(pu) = Vac(pu) \cdot \cos \alpha - Rc \cdot Idc(pu) \quad (4)$$

Thus, Qdc can be changed through firing (or extinction) angle α . In fact, for certain applications, it is desired that the converter at no load continues the commutation process in order to control its ac bus voltage. In such circumstances, firing angle α can approach steady state values near 80°. This necessiates that the dc converter valves and their damping and cooling circuits are designed to accommodate the operation at high firing angles. The additional incremental capital investment in the dc terminal converters and filters required for such application, however, can be only a fraction of the total capital and operational costs associated with the other solutions.

When the HVDC converter is of a rating comparable to the ac system short circuit capacity (i.e. low SCR), changing Qdc can have an appreciable impact on the reactive power balance at the ac/dc interconnecting point. Consequently, ac voltage control is more effective.

Fig. 7 shows the proposed control scheme for an HVDC converter. In normal operation the converter operates in either constant current mode (rectifier) or constant extinction angle mode (inverter). When the ac terminal voltage experiences any deviation from its set value, the output of the ac voltage regulator overrides other outputs. Newly generated thyristors firing angle will immediately change the amount of reactive power absorbed by the dc terminal in such a way to control the ac voltage to its pre-set value. During this process, the other HVDC converter terminal will automatically take over the dc current control. Both dc converter terminals will then be running at comperative firing and extinction angles and consequently drawing the same order of magnitude of reactive powers. This, however, should not be of real concern since the dominant control action is to correct the voltage on the weaker ac side of the HVDC terminals. Therefore, the impact on the other relatively stiffer side is minimum. Also, when a temporary overvoltage occurs at one point, simultaneous overvoltages with different magnitudes appear at other points in the interconnected ac network. When the dc link is connected in parallel with other ac lines, changing the reactive power absorbed by both dc terminals will be highly beneficial.

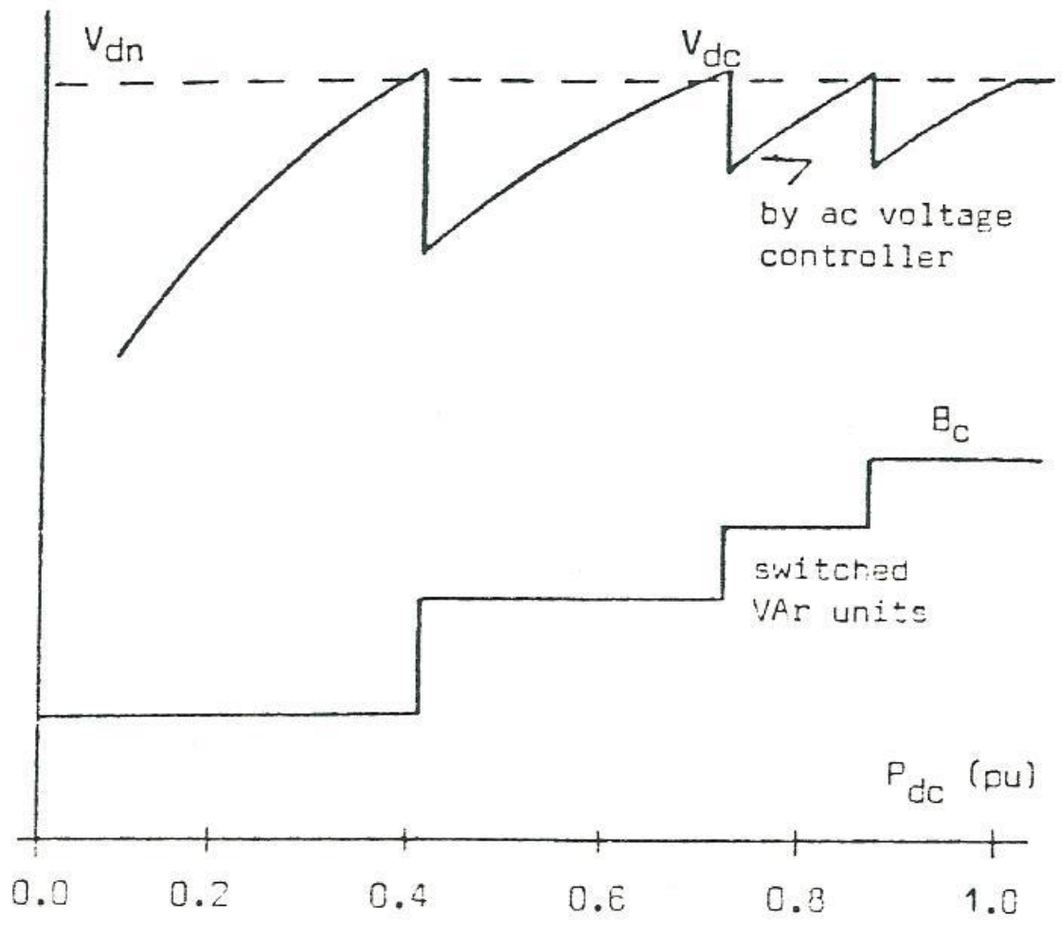

Fig. 8 Coordination between ac voltage controller and switched VAr units of a HVDC converter terminal

To accommodate slower voltage variations and to keep the operating dc voltage close to its nominal value, coordination with switched VAr units (e.g. capacitors, reactors and filter banks) is necessary. This is illustrated in Fig. 8 for different dc power levels. For this purpose the controllers, integrated in the microprocessor based converter controls[11], must possess a hysteresis type characteristics in order to avoid undeterministic switching positions.

When dynamic overvoltages appear at the ac terminals, the HVDC converter ac voltage local controller is actuated. The converter firing angle (in case of rectifier) or extinction angle (in case of inverter) will increase . Such a control action results in a fast and continuous (smooth) variation of converter reactive power. Under these conditions, the high inverter extinction angles will always ensure a reliable dc operation in the weak ac system without the risk of repetitive commutation failures. At the points when the dc voltage exceeds a certain low limit - dedicated by overall system conditions - signals are released for sequential switching of reactive power units. These switching actions are used primarily to ensure operation close to the nominal dc voltage, thus insuring minimum system losses. They also provide the necessary Q-bias to supplement the controls to completely eliminate all dynamic over and under voltages.

Taking all these factors into consideration, the size of each switched VAr unit can be further optimized, thus allowing for more economic choice of the HVDC terminal layout.

TRANSIENT PERFORMANCE OF PROPOSED TECHNIQUE

Figs. 9 and 10 show the HVDC simulator results of the transient recovery process of an HVDC scheme following various faults at either one of its terminals.

A 3-phase short circuit fault is simulated on one ac line terminated at the HVDC rectifier terminal. The fault is assumed to be cleared in 6 cycles by opening the ac line without reclosing. The pre-fault short circuit ratio is 2.4 and subsequent to fault clearing SCR is 1.6.

Two control schemes are separately simulated: Fig. 9 illustrates the first scheme in which sequential switching of reactive power units is utilized without the ac voltage regulator. When the low ac voltage at the HVDC terminal is detected, all switchable capacitor banks and a filter (total 0.7 pu) are switched off (4 cycles after fault initiation) in anticipation of the high recovery voltage. One filter bank is left for appropriate dc restart. The HVDC is blocked in one cycle and de-blocked in two cycles after fault clearing. High overvoltage is experienced after clearing the fault with a peak of 1.7 pu. Following the dc power ramping, the filter and capacitor banks are sequentially switched back on.

Fig. 10 shows the results for the second scheme with the ac voltage regulator. In this case, the HVDC converter is allowed to continue firing, instead of being blocked, during the fault period. Without switching any of the reactive power units, the HVDC scheme is able to limit the recovery overvoltage (first peak is 1.25 pu) and successfully ramp back to its full operation. This is achieved by the fast control action of the ac voltage regulator acting on the rectifier firing angle in this case. As shown in Fig. 10, the ac voltage magnitude is effectively and quickly controlled back to its prefault 1.0 pu value.

Of course, when this control action is coordinated together with the switching operations of the reactive power units, the results would be significantly further improved due to the combined effects.

Other severe fault conditions have also been studied when the dc terminal is operating in either rectifier or inverter mode. When the proposed ac voltage control technique is adopted, the overall system transient response was similar to that shown in Fig. 10.

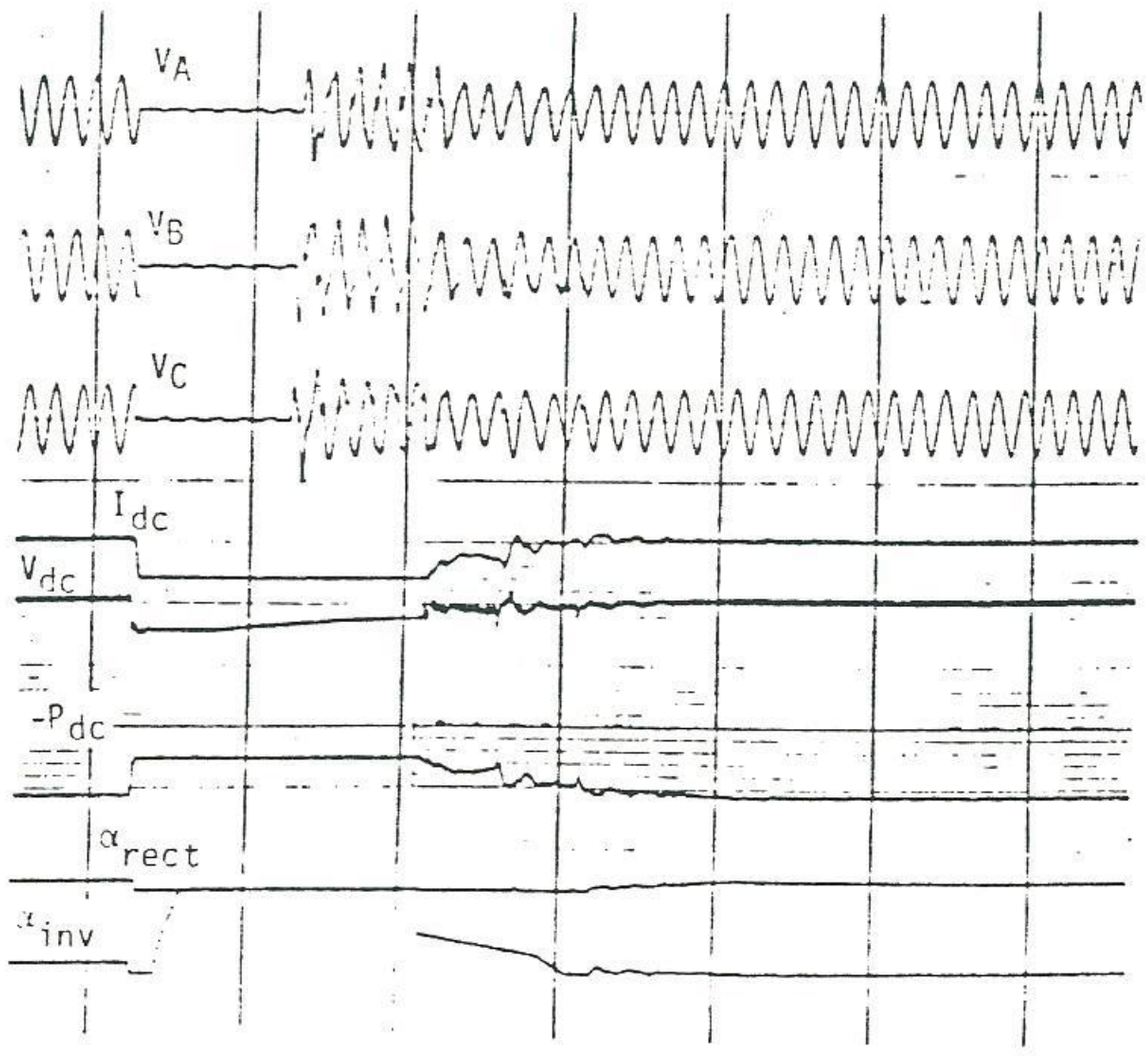

Fig. 9 System transient response for ac line 3-phase short circuit near rectifier cleared in 6 cycles by opening the line (SCR=1.6). With sequential switching of reactive power units

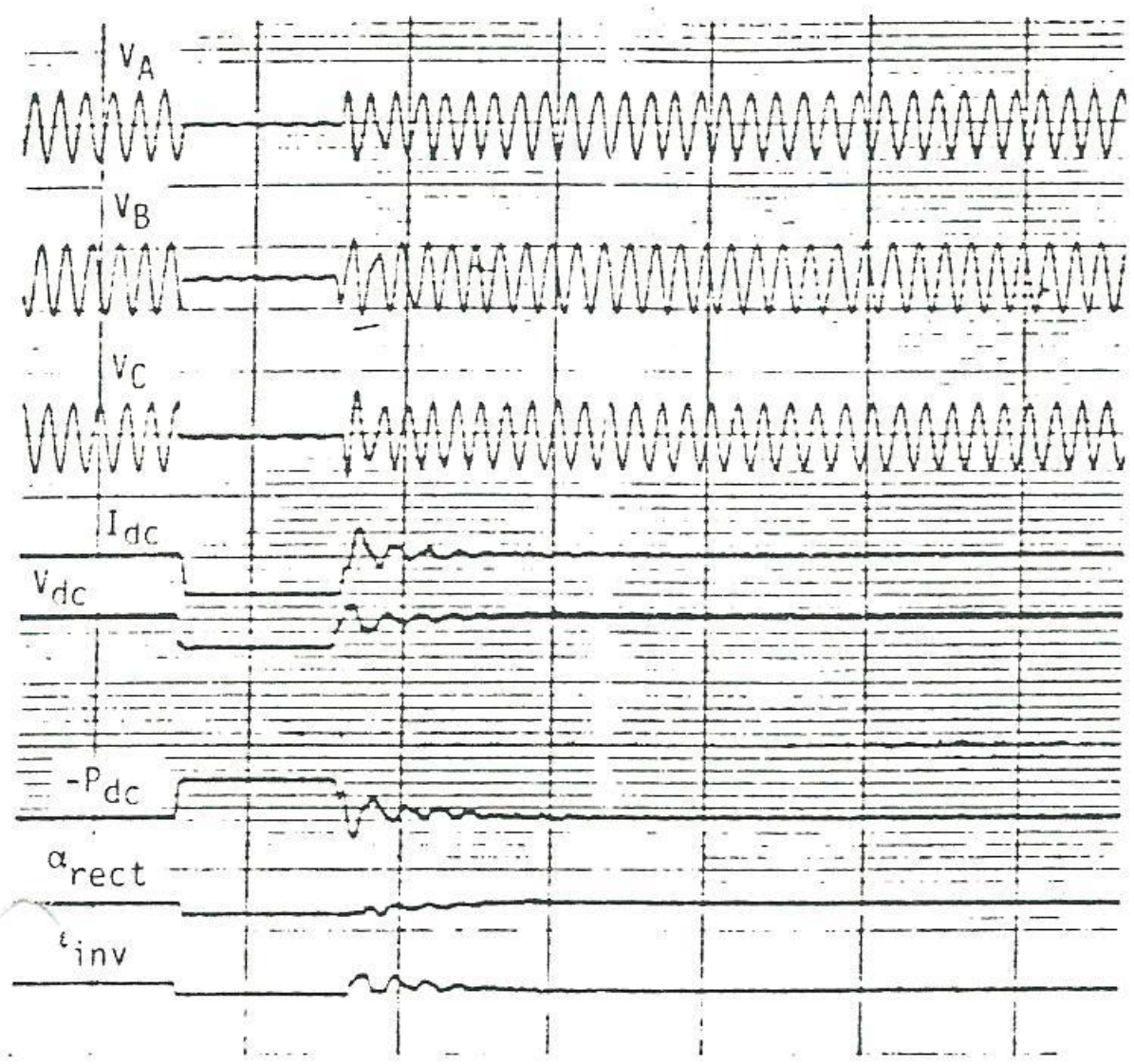

Fig.10 System transient response for ac line 3-phase short circuit near rectifier cleared in 6 cycles by opening the line (SCR=1.6). With HVDC ac voltage controller. No capacitor switching.

COMPARISON WITH OTHER VAR CONTROL TECHNIQUES

To further demonstrate its technical merits, the proposed technique is compared to other known methods for voltage or reactive power control; namely, synchronous condensers and static VAr compensators. The comparison is carried out by the aid of digital time simulations of the fundamental frequency behaviour for the comprehensive ac/dc system model.

The same system as discussed before where original short circuit ratio at the ac/dc interconnection point is 2.4 , is studied. Synchronous condensers of 0.7 pu rating are added at the HVDC terminal to replace the switched reactive power units. The synchronous condensers are assumed to have a total transient reactance of 35% and step-up transformers of reactance 15% based on their own rating. This will contribute an additional short circuit capacity of 1.4 pu at the HVDC terminal. The effective SCR is therefore increased to 3.8. A 3-phase short circuit fault is simulated on the ac side of the dc converter station. The fault is assumed to be cleared in 7 cycles by tripping one ac line thus reducing the SCR to 2.0 . During the fault period the HVDC converter is blocked and is ramped back to its prefault operation after fault clearing as shown in Fig. 11. The ac terminal voltage Vac is shown with a recovery peak overvoltage of 9%. However, following complete recovery of the HVDC, voltage and power fluctuations of + 2% and + 0.12 pu respectively take place at the terminals of the synchronous condensers. This is primarily due to the rotor oscillations of synchronous condensers on account of their inertia following the disturbance.

If static VAr compensators - thyristor controlled reactors TCR - with rating 0.35 pu, are employed instead, the switched VAr units (capacitors in this case) are also utilized. Controls of the combined scheme are driven by the variations of both voltage and reactive power at the HVDC terminal. As in the previous case, the dc is blocked during the 3-phase short circuit and allowed to recover after fault clearing. This is illustrated in Fig. 12. During the fault period, the TCR is forced to be fully conducting and capacitor and filter banks of 0.35 pu are switched off in order to reduce the recovery overvoltages. After fault clearing the peak dynamic overvoltage is 9.3%. The HVDC, the ac voltage and the power flow on the ac lines fully recover to pre-fault conditions in about 100 ms. As the dc power ramps up, the switched capacitor and filter banks are switched back on sequentially. The reactive power absorbed by the TCR is also shown in Fig. 12.

When the proposed technique of ac voltage control by the HVDC converter is used, the converter valves are kept conducting during the fault period. In anticipation of the high recovery temporary overvoltages,

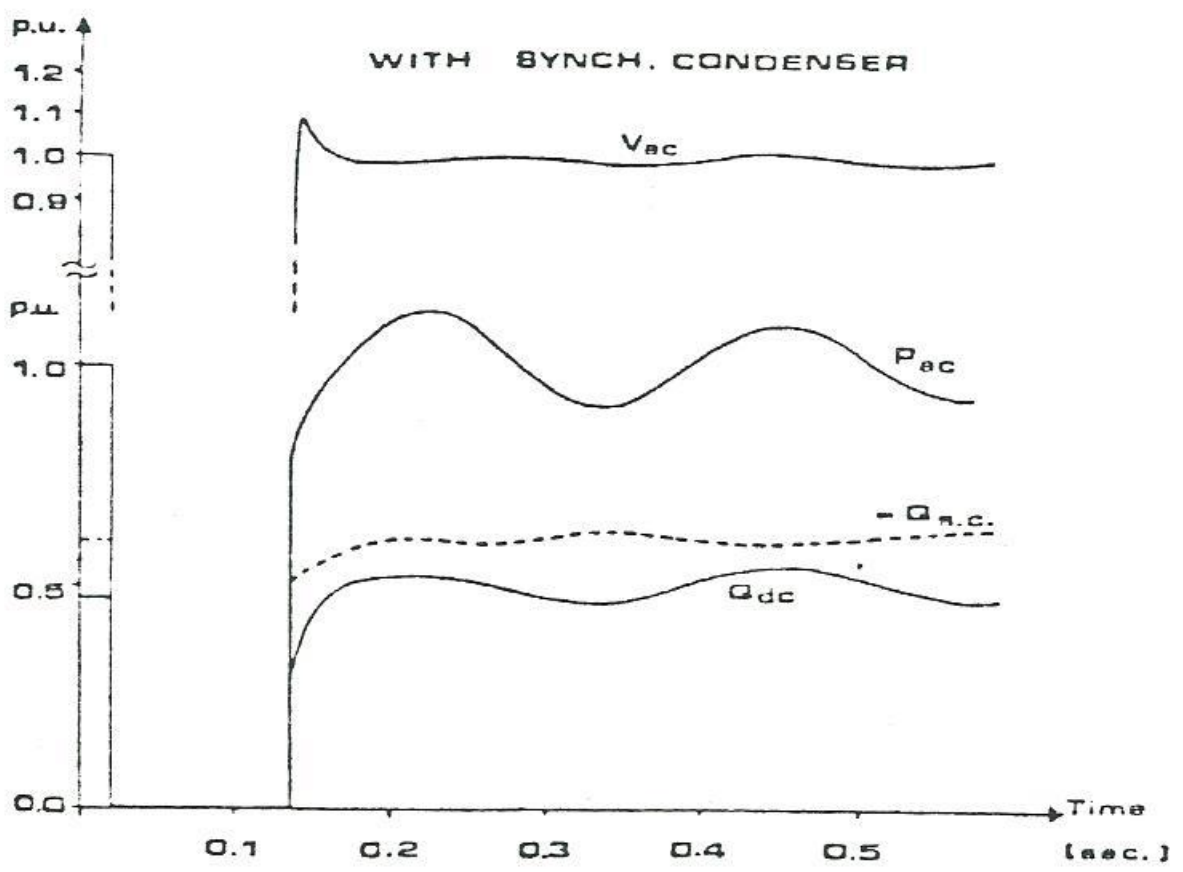

Fig.11 System fundamental frequency response for 3-ph. short circuit at HVDC terminal (7 cycles). With synchronous condensers (0.7 pu rating)

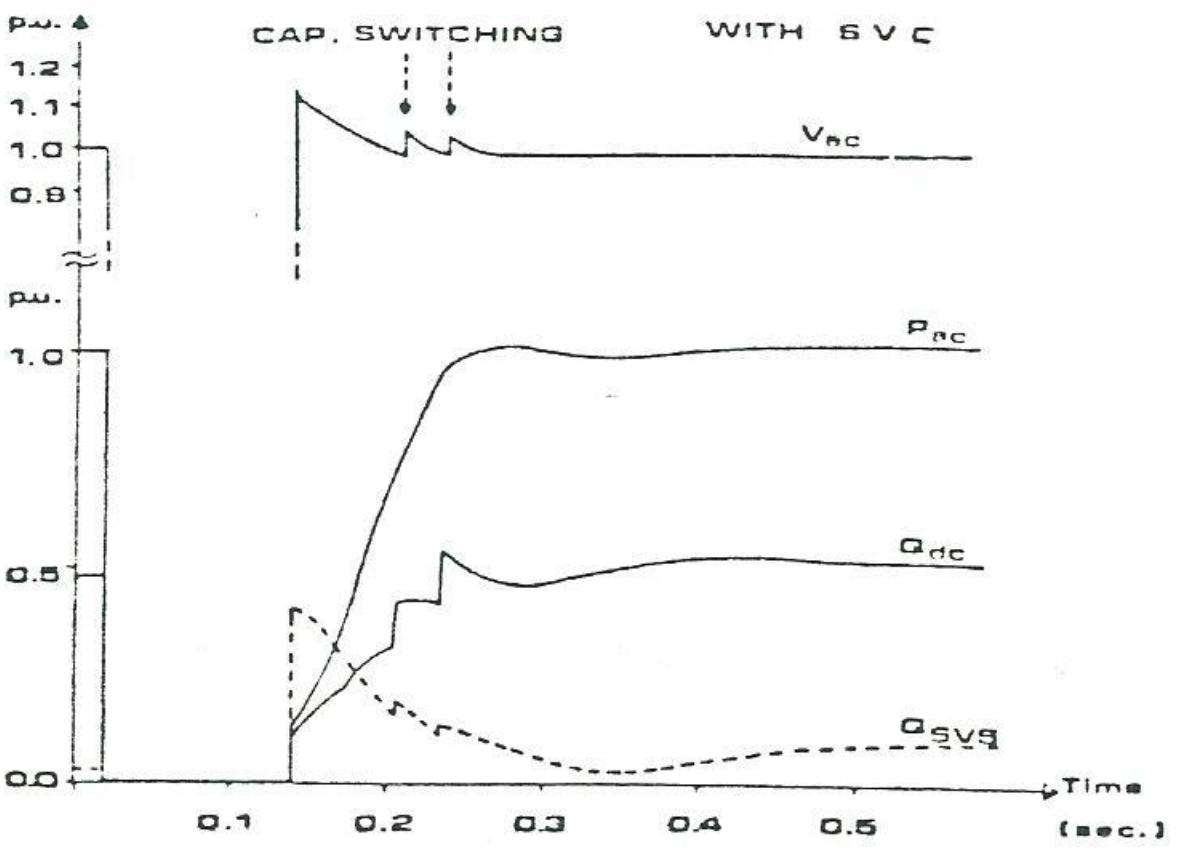

Fig.12 System fundamental frequency response for 3-ph. short circuit at HVDC terminal (7 cycles). With static VAr compensators (0.35 pu rating) and capacitor switchings

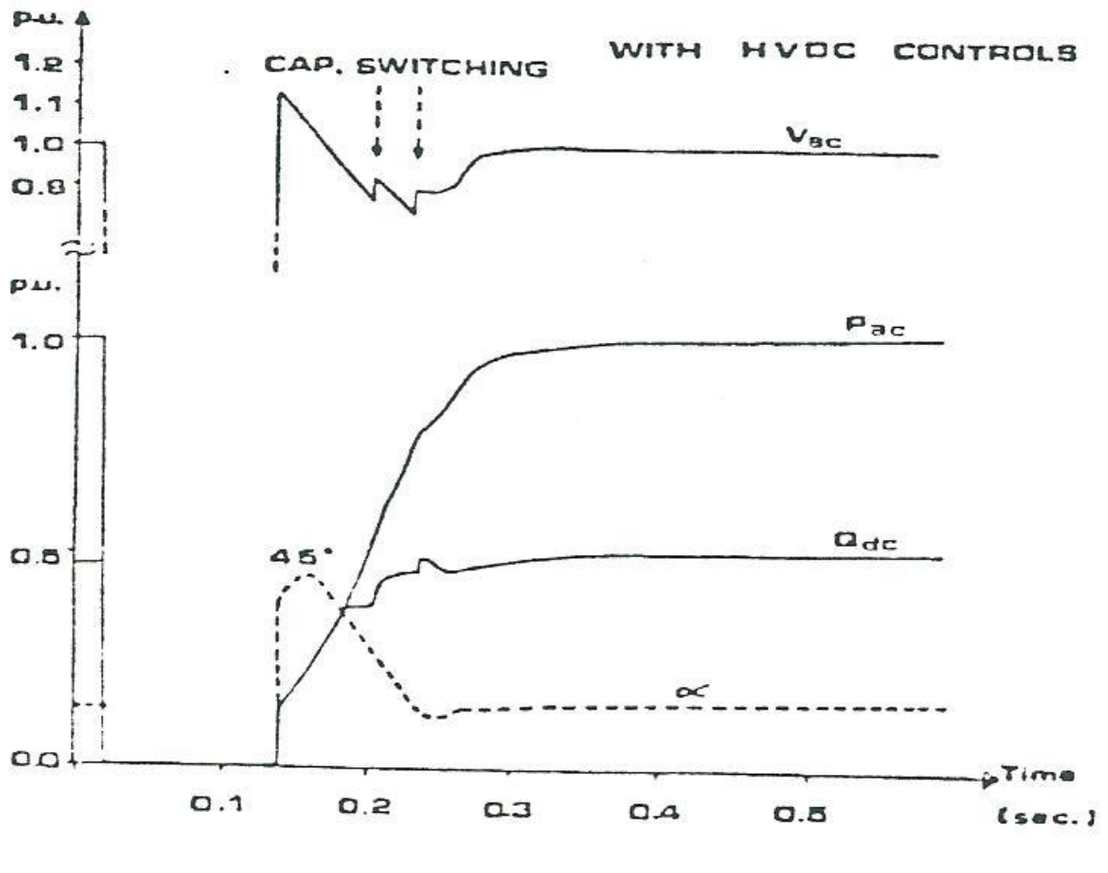

Fig.13 System fundamental frequency response for 3-ph. short circuit at HVDC terminal (7 cycles). With ac voltage controller of HVDC and cap. switching

capacitor units of 0.525 pu are switched off and rectifier firing angle is kept high. The recovery overvoltage in this case, as shown in Fig. 13, is 12.5% but the ac voltge quickly drops as the HVDC is ramped back. To counteract the high dynamic overvoltage, the reactive power absorption of the dc converter terminal is increased by means of the high firing angle shown in Fig. 13. The dc voltage in this case is temporarily reduced, thus causing a short delay in the post-fault recovery of the converter dc power. Following the dc power partial recovery accompanied by low ac and dc voltages the capacitor banks are sequentially switched back on. The ac voltage is controlled to 1.0 pu and the dc power recovers to its pre-fault value as well as the power flow on the terminated ac lines.

It is worth noting that while the synchronous condensers produce oscillating power flows on the interconnected ac lines, such oscillations do not take place with static VAr compensation or static voltage control methods. On the other hand the delay in the recovery of the dc terminal power after fault clearing on account of the temporary reduction of the dc voltage associated with the proposed technique is almost insignificant. Compared with static VAr compensators, the delay is only in the order of one to two cycles. Also regarding the overall system losses, the voltage regulation technique by the HVDC converter controls proved to be more economically attractive. Relatively high losses are associated with synchronous condensers and thyristor controlled reactors as well as their step up transformers - when operated at full loads. Therefore, considerable savings in the overall system losses can be achieved even when the HVDC scheme is temporarily running at low dc voltage levels.

CONCLUSIONS

An advanced scheme for controlling the ac voltage at the terminals of HVDC schemes has been presented. The objective of this new technique is to fully utilize the dc converter itself without physically or artificially increasing the ac system short circuit capacity, thereby making HVDC schemes more economical. This is realized by regulating the reactive power absorption of the HVDC terminal, during steady state and transient conditions, through a local controller added to the thyristors firing angle controls.

Coordination with the switched reactive power units and filters, usually installed at the HVDC terminal, supplements the voltage regulation function of the proposed technique and insures operation with optimized system losses.

The voltage stability criterion, derived from the linearized model of combined ac/dc system, has been utilized to determine the regions for potential ac voltage instability at the ac/dc junction. The alternative solutions for ac voltage control problems have been examined using this criterion.

Comparison with other schemes for voltage control, such as synchronous condensers and static VAR compensators, has been demonstrated by digital and analogue simulations of the complete non-linear ac/dc system under various transient operations. The performance of the new technique proved to be superior even under low short circuit ratio conditions.

REFERENCES

[1] R.E. Harrison, "Type, Significance and Control of Overvoltages at the Junction of AC-DC Systems", Overvoltages and Compensation on Integrated AC-DC System Conference, Winnipeg, 1980, pp. 1-4

[2] J. Käuferle, K. Sadek, D. Povh, "System Aspects of the Application of static VAr Systems at AC Bus of HVDC system", Overvoltages and Compensation on Integrated AC-DC System Conference, Winnipeg, 1980

[3] J. Käuferle, et.al., "HVDC Stations Connected to Weak AC Systems", IEEE Trans. Vol. PAS-89, No. 7, 1970, pp. 1610-1617

[4] K. Kanngiesser, P. Lips, "Control Methods for Improving the Reactive Power Characteristics of HVDC Links", IEEE Trans. Vol. PAS-89, No. 6, 1970, pp. 1120-1125

[5] J. Käuferle, C. Beriger, "Possibilities to Control the AC Busbar Voltage by Reactive Power of an HVDC Terminal", IEE Conference, Publication No. 107, 1973, pp. 75-79

[6] A. Hammad, D. Woodford, R. Mathur, "AC Voltage Control at an HVDC Terminal", Canadian Communication & Power Conference, Montreal 1978, pp. 341-344

[7] C. Grund, R. Pohl, J. Reeve, "Control Design of an Active and Reactive Power HVDC Modulation System with Kalman Filtering", IEEE Trans., Vol. PAS-101, Oct. 1982, PP. 4100-4111.

[8] A. Gavrilovic, "HVDC Infeed into Relatively Weak AC System", CIGRE SC- 14, Vienna, June 1983.

[9] K. Reichert, et.al., "Network Analysis Programs, Methods and Studies for Solving Power System Problems", Brown Boveri Review, Vol. 70, January 1983, pp. 9-12

[10] A. Hammad, J. Käuferle, "Fault Recovery of HVDC Transmission: Relevant Simulation Studies for Practical Cases", International Symposium on HVDC Technology, Rio de Janeiro, March 1983, paper 1-6.

[11] H. Stemmler, et.al., "Programmable Processor for the Control in Power Electronics", 3rd IFAC Symposium in Control in Power Electronics, Lausanne, Sept. 1983, pp. 493-500.