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— Chicago Section —

Nanoscale Chip Design

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Chicago Section Executive Committee Meeting
Tuesday, January 10, 2006, 7:00 p.m.
DeVry DuPage, Room TBA, 1221 N. Swift Rd., Addison, IL
No Registration Needed

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Nanoscale Chip Design Advancing On Many Fronts

By Paul Zukowski

Advancement in the speed and intricacy of semiconductors depends on ever-smaller devices and circuits. Yet packing more transistors and circuitry onto computer chips is challenging engineers and the materials they use.

The modern technology for etching transistors onto silicon wafers is called photolithography. Light is shone through a negative of the chip design onto photosensitive material covering the silicon. The material hardens where the light hits, but stays soft where it is dark. The hardened material is washed away with chemicals, leaving the processor's pattern. Metal is then deposited into this pattern to form the tiny wires on the processor.

The problem is that the wavelength of visible light is too large for the next generation of circuits. This has led to Intel and others developing a new method called extreme ultraviolet lithography. EUV lithography uses very short wavelengths that need reflectors made of several layers of ultra-thin silicon and molybdenum to focus the beams. These new lithography tools are expensive. Where a tool for a 193-nanometer system can cost $20 million, tools using EUV lithography can cost four times that.

Some researchers are reaching beyond the spectrum for new ways to make nanoscale circuitry. In the Aug. 30 issue of Applied Physics Letters, a team of researchers from the U.S. Naval Research Laboratory and the Georgia Institute of Technology report success using a high-tech version of the glue gun to help lay down patterns of circuits the size of molecules. The melting and placement uses a hot tip at the end of the cantilevered arm of an atomic force microscope. In about a millionth of a second, the heat of the probe can top 1,250 degrees Fahrenheit. Various metals put on the tip are heated and transferred to a surface being patterned in layers as thin as one molecule. Through alternate heating and cooling, the deposition of the material can be precisely controlled.

This technology is called thermal dip pen nanolithography, and is an extension of regular dip pen nanolithography that is used to draw circuits. The thermal technique is seen as useful for several applications, including repair of very expensive semiconductor masks. The technique might also prove highly useful for rapid prototyping of nanoscale materials. The thermal approach could also be used to build three-dimensional nanostructures with multiple components by using materials with different melting temperatures. And because the technique is compatible with vacuum environments, it may also find application in present semiconductor patterning.

New type of switch

Other researchers are looking for new ways to make electronic switches and circuits. Earlier this year, a group of researchers at Hewlett-Packard Labs in Palo Alto, Calif., reported creating a molecular-scale alternative to the transistor that could produce ultrasmall electronics beyond what is possible with silicon-based technology.

In an article in *The Journal of Applied Physics,* researchers described how they designed a "crossbar latch" only a few atoms across that can be programmed by a repeatable set of electrical pulses making it possible to perform the type of on/off logic operation essential to computer functions now done by transistors.

The Hewlett-Packard team was able to create the nanoscale switches using a mesh of molecular-sized wires that overlap, creating contact points at each overlapping junction. They began to focus on molecular electronics a number of years ago when it became clear that existing semiconductor manufacturing techniques would eventually limit how small the transistors could be.

The crossbar approach is becoming widely used among researchers because its components are relatively simple to fabricate and can achieve striking densities,

continued on page 4…

packing one trillion crossbar junctions in a square centimeter. Rather than relying on conventional photolithography, researchers in molecular electronics are using an alternative approach known as imprint lithography, which relies on ultrafine molds to create overlapping wire grids.

Shrinking the transistor

Other researchers are not giving up on the transistor yet. In fact, New York State officials announced a $600 million partnership with the computer industry this summer to develop technology at the State University at Albany to make transistors even smaller. The project is called the International Venture for Nanolithography, and one of its goals will be to shrink transistors to 22 nanometers from the present limit of 90 nanometers.

The project will get $200 million in funding and equipment from four high-tech companies: IBM Corp., Armonk, N.Y.; Advanced Micro Devices Inc., Sunnyvale, Calif.; Infineon Technologies of Germany; and Micron Technology Inc., Boise, Idaho. New York State is contributing another $180 million. An additional $200 million-plus is coming from several companies that provide the materials and equipment used to make semiconductors. Not involved is Intel Corp., which accounts for about 80% of worldwide sales of microprocessors by unit volume and 90% by revenue.

New York Gov. George E. Pataki has made a major effort of his administration to lure businesses and investors to Albany NanoTech, the research operation based at the State University at Albany. Earlier Pataki had helped lure Sematech, the computer chip consortium that helped transform Austin into a major center of computer research, to Albany. Since then, several other big companies have been lured to the area. Now the focus is on lithography, using smaller and more focused wavelengths of light to etch smaller and smaller patterns onto semiconductor materials to create circuits. Since the Sematech deal, the state has given $535 million to start projects at Albany NanoTech, and private industry has committed to investing $1.7 billion. There are currently about 645 people working at NanoTech, and the new project is expected to bring more than 200 more jobs.

Pinpointing atoms

Engineers at the University of Wisconsin-Madison have demonstrated a way to chart semiconductors on the scale of atoms. In a study published in the August issue of Applied Physics Letters, researchers describe using a local electrode atom probe (LEAP) microscope to pinpoint individual atoms of boron, a common dopant used to control the electrical properties of silicon transistors. The paper explains that for atomic-scale transistors to function properly, boron must be implanted at very high concentrations within the first 200 to 300 atomic layers of the silicon surface.

The LEAP microscope can analyze roughly 50 million atoms an hour and map the properties of even the tiniest semiconductor devices, atom by atom. And for devices below the 100-nanometer range knowing where are all the individual atoms and what type of atoms are they becomes crucial.

LEAP is an advanced atom probe microscope invented by Tom Kelly, a former UW-Madison professor of materials science and engineering, who left the university to start Imago Scientific Instruments and produce LEAP. It works by applying voltage to a specially prepared, needle-shaped sample, ripping atoms from the sample's tip one by one. An electric field then pulls the charged atoms to a detector, which identifies them and records their location in the original specimen.

These and other developments are pushing the limits of electronic circuitry ever smaller and ever faster, and will continue to transform the field in the future. ■

Evening Meeting

Chicago Chapter of the IEEE Power Engineering Society

Underground Medium and High Voltage Cables

Wednesday, January 11, 2006

Jim Fitzgerald
The Okonite Company

About the Topic:
Join Jim Fitzgerald on a technical journey covering medium and high voltage cables from beginning to end. Specific stops along the way will include:

- Industry Standards
- Medium and High Voltage Cable Design
- Cable Manufacturing Processes
- Qualification and Routine Production Testing

About the Speaker:
Jim Fitzgerald is currently the Vice President-Application Engineering for The Okonite Company. His current responsibilities include: internal company standards, Qualification reports, technical support for Sales and customer data requirements. Jim graduated from Manhattan College in 1970 with a Bachelor of Science degree in Electrical Engineering. He is presently the Vice Chair/Treasurer of the Insulated Conductors Committee of the IEEE Power Engineering Society. He is a member of UL's Standards Technical Program and is a member of Committee 38 of the AREMA Railroad standards group.

Location:
ComEd Commercial Center, 1919 Swift Drive, Oak Brook, IL (near the I-290 and I-294 interchange)

Time:
5:30 Social
6:00 Dinner (optional)
6:45 Presentation
8:00 Adjourn

Continuing Education:
IEEE technical meetings may be acceptable as continuing education where required for maintenance of professional engineering licensure. Refer to the individual state's requirements for details.

Reservations:
Please call the IEEE Business Office by noon on Monday 9 Jan 2006 at (630) 493-4333 or (800) 898-IEEE to make your reservation. Or, submit your data via the Online Reservation Form.

Cost:
The cost of the optional box-lunch style dinner is $15 for IEEE members, $20 for non-members, payable at the event. Sorry, we are unable to process credit cards. Checks payable to "IEEE-PES Chicago Chapter" and cash are accepted, and receipts will be provided.

For more information:
For more information, including the Online Reservation Form, please visit the IEEE PES Chicago Chapter web site: http://peschicago.org

Where do Engineers Come From?

Oaks come from acorns. Butterflies come from caterpillars. It's not quite as obvious where Engineers come from.

Engineers come from curiosity. They come from a desire to improve things. But, most of all Engineers come from knowledge – especially at an early age. Sometimes the best engineering students are the most unlikely. Their parents may not be engineers. They may not even know any engineers. But they have an intellectual curiosity into how things work and strive to craft solutions to make things work better.

Locating these potential engineers and presenting the potential of an engineering education is the purpose of the National Engineers' Week activities. Math Counts, Jets Teams, and Model Cities are slanted to give those students who already had that interest sparked an opportunity to start participating in engineering-oriented activities.

For those students who still equate engineers with large trains, there is the National Engineers Week Expo to be held February 25 at IIT Rice in Wheaton. (http://www.rice.iit.edu/engineersweek/).

Hands-on activities, displays, and presentations will highlight the various contributions of engineers. Engineers from numerous disciplines will be on hand to answer the students' questions. Elementary and High School students will be able to see the impact engineering has on their lives. Since the National theme for Engineers' Week is Women in Engineering, the contribution of women will be highlighted. As always, all of the workshops, displays, and presentations are completely free to the students.

IEEE Chicago Section supports this worthy endeavor. From touchable equipment to a working ham station, Chicago Section has had displays to show the students how Electrical and Electronics Engineering touch their lives. Several members of the section staff the booth to field questions. (IEEE members who would like to participate in bringing EE to the students in an interesting and vibrant manner are encouraged to contact ckelly@ieee.org.)

Mark your calendars FEBRUARY 25 – IIT-RICE Campus – National Engineers Week Expo! ■

Dinner Meeting

IEEE – IAS/IES Dinner Presentation

Medium Voltage Cables

Wednesday, January 18, 2006

Carroll Lindler, PRYSMIAN Power Cables and Systems USA
Present Position: Product Manager/ Sr. Applications Engineer

About the Topic:
Extruded, solid dielectric insulated power cables have been in use in the United States for over forty years in utility and commercial applications. These cables have incorporated numerous types of insulations; HMWPE, XLPE, TRXLPE and EPR come to mind as the most common. Different insulations have various electrical and physical characteristics, advantages and disadvantages. This presentation will provide useful information on the basics of the two most common insulations, TRXLP and EPR, while touching on XLPE as well. Further, the presentation will cover water-blocking technology that is the equalizer for these insulation compounds. Lastly, new technology in armored cables will also be presented.

About the Speaker:
Carroll E. Lindler, Jr. received his Bachelor of Science degree in Electrical and Computer Engineering from the University of South Carolina in 1991. After graduation he held Product Engineer and Design Engineer positions with Kuhlman Electric Corporation and ABB in the field of Instrument Transformer Design. Presently, he is the Senior Applications Engineer and Product Manager for Prysmian Power Cables and Systems. His responsibilities with Prysmian include numerous aspects of low voltage and medium voltage power cable design from manufacturing to installation as well as various calculations and applications duties. He is presently an active member of the ICEA.

Location:
COSTA'S (GREEKTOWN)
340 S Halsted St., Chicago, Illinois
Costa's is located in Greektown on the corner of Van Buren and Halsted.

Time:
Social 5:30 p.m.
Dinner 6:00 p.m.
Presentation 7:00 p.m.

Cost:
Your cost includes the presentation and a four-course dinner with a choice of the main entry - Roast lamb, Chicken, or Fish. (Vegetarian or special dietary meals available upon request). Cost is $25 IEEE Member and $30 non-member. Valet parking is included with your meal.

Reservations:
Please call the IEEE Business Office at (800) 898-IEEE or (630) 493-4333 with your reservation. Please note any special meal requests at the time of the reservation.

Continuing Education:
For P.E. licenses that require continuing education for renewal, attendance at IEEE Technical Meetings is acceptable as one Professional Development Hour (PDH) per meeting.

Dinner Meeting

IEEE Fox Valley Subsection

Solar Energy: Challenges and Opportunities

Wednesday, January 18, 2006

George W. Crabtree,
Argonne National Laboratory

About the Topic:
The global demand for energy will double by 2050 and triple by the end of the century. Our existing energy sources, fossil, nuclear and renewable, all face major challenges in supplying the additional energy needed for the next 50-100 years. Possible routes for producing the needed energy will be analysed, with emphasis on the basic research breakthroughs that will enable sunlight to provide a significant fraction of our future energy needs.

About the Speaker:
George Crabtree is a Senior Scientist at Argonne National Laboratory and Director of its Materials Science Division. He holds a B.S. in Engineering from Northwestern University and Ph.D. in Condensed Matter Physics from the University of Illinois at Chicago, specializing in the electronic properties of metals. He has won numerous awards, most recently the Kammerlingh Onnes Prize for his work on the properties of vortices in high temperature superconductors. This prestigious prize is awarded only once every three years; Dr. Crabtree is its second recipient. He has won the University of Chicago Award for Distinguished Performance at Argonne twice, and the U.S. Department of Energy's Award for Outstanding Scientific Accomplishment in Solid State Physics four times, a notable accomplishment. He has an R&D 100 Award for his pioneering development of Magnetic Flux Imaging Systems, is a Fellow of the American Physical Society, and is a charter member of ISI's compilation of Highly Cited Researchers in Physics.

Dr. Crabtree has served as Chairman of the Division of Condensed Matter of the American Physical Society, as a Founding Editor of the scientific journal Physica C, as a Divisional Associate Editor of Physical Review Letters, as Chair of the Advisory Committee for the National Magnet Laboratory in Tallahassee, Florida, and as Editor of several review issues of Physica C devoted to superconductivity. He has published more than 400 papers in leading scientific journals, and given approximately 100 invited talks at national and international scientific conferences. His research interests include materials science, nanoscale superconductors and magnets, vortex matter in superconductors, and highly correlated electrons in metals. Most recently he served as Associate Chair of the Workshop on Basic Research Needs for the Hydrogen Economy organized by the Department of Energyís Office of Basic Energy Sciences, which is the subject of his presentation at the OSTP briefing on Hot Topics in Science and Technology: Energizing our Future.

Location:
IIT's Rice Campus, 201 East Loop Road, Wheaton, Illinois.

Take Rt.56/Butterfield Rd. to first stoplight east of intersection of Butterfield & Naperville roads. Turn north onto East Loop Road (Philips 66 Gas Station on the corner); the campus will be on your right about a block north of Butterfield Road.

More detailed directions and a map are available at http://www.rice.iit.edu/directions.html

Time:
6:00 p.m. Networking time
7:00 p.m. Presentation

Continuing Education:
Professional Engineers: this meeting qualifies for Professional Development Hours

Reservations:
Reservations are not required.

For more information:
The Fox Valley subsection web page is at www.ieee.org/foxvalley/

Evening Meeting

IEEE Chicago/Rockford Consultants' Network

To be determined...

Monday, January 23, 2006

Thomas J. Tobin, S&C Electric Co.

About the Topic:

The Network will be holding its next bi-monthly meeting on Monday January 23, 2006 from 7:30 PM to 9:15 PM at the Palatine Public Library. We are still determining our topic and an associated facilitator or speaker. This selection will be influenced by the outcome of the December AICN Consultant's Workshop.

You are invited to obtain specifics on the topic and facilitator / speaker by visiting our web site after January 2, 2006. That web site is: www.drblank.com/coaction.htm

Members and non-members are invited to both the meeting and the optional dinner. (Reservations are NOT required).

Dinner Location:

Bakers Square. 270 E. Northwest Highway (at the corner of North Court St.), just south of the library

Meeting Location:

Palatine Public Library
700 North Court • Palatine, IL
847-358-1216

Time:

6:15 p.m. Optional Group Dinner at Bakers Square (Order off the menu – reservations not required)
7:30 p.m. Meeting – Discussion
9:15 p.m. Adjourn

Continuing Education:

We anticipate that our topic will qualify for PDH credit. In that case, attendance at this meeting will earn 1.0 PDH.

For more information:

Information about the network can be obtained by e-mail to either consultnet@bmillerengineering.com or JAuer Consulting@worldnet.att.net, or visit our web site at www.drblank.com/coaction.htm

See you on January 23, 2006, and bring consultants and those who aspire to be consultants for a pleasant and informative evening of networking.

Meetings are usually held on the last Monday of odd-numbered months.

Call for Participation NetSecure 06

IIT/IEEE Security Workshop & Expo

We invite you and your organization to participate at the 4th Annual Computer and Network Security Workshop and Expo on Wednesday, March 8, 2006. The event will be held at Illinois Institute of Technology's (IIT) campus in Wheaton, Illinois and will be co-hosted by IIT's Center for Professional Development, the IEEE Communications Society, IEEE Fox Valley and UniForum Chicago.

The workshop will bring together knowledgeable security practitioners and responsible executives from organizations such as computer and network technology providers and manufacturers, scientific laboratories, law enforcement, healthcare, and legal organizations to discuss and share their security needs, problems, technologies, security systems, plans and much more. Subject matter experts will offer technical sessions, tutorials and vendor sessions. Businesses will have the opportunity to exhibit. The event is open to the public.

The last workshop, held in April 2005 was attended by nearly 200 with representatives from many organizations, such as Avaya, Beyond If Technologies, Checkpoint Software, Cisco, College of DuPage, CompTIA, Fermi National Accelerator Lab, IEEE, Illinois Institute of Technology, IP3 Inc, IT Outpost, Kane County Government, Kent College of Law, KPMG, Modularis, NCSA, Novell, Rosetta Wireless, UniForum, Wheaton College, and many more.

Topic areas include but are not limited to computer and network security including spam & phishing prevention, privacy, regulations (e.g., HIPAA and Sarbaines-Oxley), computer and network crime investigation and forensics including chain of evidence, steganography, criminal and civil concerns.

There are several ways you and/or your organization can participate:

Presenter – present a topic and/or a tutorial in computer and network security - topic recommendations are being accepted

Sponsor – become an event sponsor (opportunities include breakfast, lunch and wine & cheese sponsorship and raffle prizes and giveaways)

Session Organizer – organize a session on a security topic. Identify/invite the speakers and pull together the session and moderate it

Exhibitor – promote your business with a table-top "booth", Internet access and poster area

Attendee – attend the event

Tutorial – opportunities exist for tutorials adjacent to the workshop.

If you or your organization are interested in participating, please visit our web site at http://www.cpd.iit.edu/netsecure06 or email netsecure06@iit.edu. ■

Successful Career Planning Conference a Big Hit

By Doug Staszesky

On November 12, 2005, the IEEE Chicago Section hosted a Members Professional Activities Conference (MPAC) to help IEEE members work on career development and planning. The Conference was sponsored by S&C Electric Company, IEEE – Region 4 and the IEEE – Chicago Section.

Figure 1 Conference Attendees

John Zulaski, IEEE Chicago Section Vice-Chair organized the event with the able help of his committee – Marc Balban, Pat Hutson, Bill Nartker and Safoora Fatima.

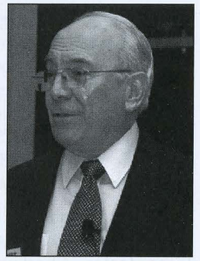
When asked why he developed the conference, John said "As I got more involved in the Chicago Section, I realized an MPAC Conference would be a great way to help our constituents deal with the impact of outsourcing, offshoring and other factors that are affecting employment of electrical engineers in the Chicago area."

John's vision is timely. Today's world is rapidly flattening through technology. The bursting of the internet bubble left a glut of high-speed fiber communication channels to many countries, which, in turn, allows work to be "offshored" to India, China and other countries. Many of these other countries focus their best and brightest in the engineering fields and work hard to bring in work from the United States. This leaves the engineer here to find new ways of enhancing their career to either keep the job they have – or find a new job inside, or outside, their current company. Some will even start up a venture based on their own intellectual capital.

The MPAC conference featured sessions on essential skill development from technical writing to public speaking to patent development to time management. All sessions aimed to help the 60 attendees enhance their skills and continue development of their careers.

Michael Wynne, President of International Management Consulting Associates, delivered a keynote speech designed to help the attendees understand not only why, but how they need to prepare for the jobs of the future – in an increasingly interconnected world.

Figure 2 - Michael Wynne - Keynote Address



Michael pointed out that China graduates over 350,000 engineers a year – orders of magnitude more than the United States. But, there is a difference between quantity and quality. And the way each person needs to differentiate him or herself is by making sure they offer the highest quality talent to employers and customers either here or abroad.

Other key points from the conference were:

- Promote your personal "brand" – go ahead and toot your horn!
- Make yourself visible – in industry associations, company committees and in your community.
- You say "I can do all these things!" Bosses and prospective employers will ask you "so what?" – be prepared to answer!
- Learn how to write and speak in public – and do it well!
- Make sure you know how to set priorities – and then do it!
- Know how to both promote and protect your intellectual property.
- Make a career plan, take action on your plan, update your plan. Planning is more important than the plan itself!

Figure 3 - Questions are Good!

This conference was a tremendous value for engineers in the Chicagoland community. The participants' evaluations showed great enthusiasm, and a future conference is being considered.

If you're interested in participating in next year's conference, contact John Zulaski at jazulaski@prodigy.net for opportunities in committee leadership, sponsorship and speaking – they'll all help you network and raise your "value proposition"! Also, if you did not have the opportunity to attend the Conference and would like a copy of the presentations, call 1-800-898-IEEE. ■