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FEBRUARY 2005

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Chapter Meetings

SCV-LEOS - 2/1: **Cavity Enhanced Spectroscopy** – cavity ring-down spectroscopy (CRDS) can provide high sensitivity, high precision, and absolute calibration in a wide range of environments ... **[more]**

SCV-EMC - 2/8: **Locating ESD and other Impulsive Events by Time of Arrival**- with fast digital scopes widely available, impulsive events can be located with simple handmade antennas... **[more]**

SCV-EDS - 2/8: **Optoelectronics at Work: From Optical Inverters to Detectors** - two major on-going projects within the Center for Micro and Nano Technology at Lawrence Livermore National Labs ... **[more]**

*SCV-CPMT - 2/9***: From Printed Circuit Boards to Substrates: Reflecting on the History of these Technologies** – manufacturing challenges, development needs, environmental demands ... **[more]**

SCV-Com - 2/9: **Open Wireless Architecture (OWA) for Next Generation Wireless and Mobile Communications** - integration of different evolving and emerging wireless access technologies in a common flexible and expandable platform ... **[more]**

SCV-MTT - 2/10: **High Frequency Vector Network Analyzer Calibration Basics** - the basic theory of the VNA, its calibration, calibration standards and models, and accuracy factors ... **[more]**

*SCV-CS + Stanford - 2/10***: A RISKS-Oriented View of Software Development** - lessons to be learned from the cases collected in the Online Risks Forum and the ACM Software Engng Notes ... **[more]**

SCV-Mag - 2/15 **Spin Torque, and Nanorings** - description of two new topics in magnetic nanostructures from inception to realization to potential applications ... **[more]**

*SCV-EMB - 2/16***: On-demand Technology Development for Medical Imaging Clinical Trials** - challenges encountered in developing technology for managing imaging-based clinical trials ... **[more]**

*SCV-SSC - 2/17***: SiGe Heterojunction Bipolar Technology and Applications** - HBT's can be easily integrated into a standard CMOS flow for full-fledged manufacturing ... **[more]**

*OEB-IAS - 2/17***: Short Circuit and Coordination Analysis Studies** - helpful guidelines and advice on producing and then analyzing the computed and graphical results ... **[more]**

OEB-Com - 2/17: **Electromagnetic Interference Shielding for New Communication Products** - methods & products solve problems while at the same time complying with new mandated regulations ... **[more]**

*SCV-CNSV - 2/22***: High Tech Recovery! Is it going to be as good as it has been?** - new data on the Silicon Valley, state and US high-tech industry, for self-employed and independent consultants ... **[more]**

SCV-PACE - 2/22: **The Realities and Myths of Engineer Retraining** - industry and education panel with views for working engineers **[more]**

SCV-PSES - 2/22: **Effective Environmental Stress Screening, and Lab Tour** - how to effectively apply ESS to your products, and tour of Quanta Labs ... **[more]**

SCV-CPMT - 2/24: **High Frequency Fullwave Simulation of Packages** ... **[more]**

SCV-MBS - 2/26: **Radiofest: Public Service Event for Demonstrating Science and Technology for the Public Welfare** – free event includes many 1-hour talks, plus demonstrations of radio modes, and a vendor fleamarket **...** **[more]**

Upcoming Conferences

27 Feb – 4 March: **Microlithography Symposium**
San Jose Convention Center **[more]**

6-10 March: **Embedded Systems Conference**
Moscone Convention Center, San Francisco **[more]**

March 9-11: **Int'l Symposium on Systems and Human Science - Safety, Security, Reliability**
Milbrae (Westin at SF Airport) **[more]**

21-23 March: **Symp on Quality Electronic Design**
Double Tree Hotel, San Jose **[more]**

Upcoming Courses in the Bay Area

Feb 15: **Clear Business and Technical Writing**
Feb 18: **Presentation Skills for Engineers**
Feb 24: **Writing Effective E-mail Msgs** **[more]**

March 8: **Communication & Conflict Mgmt using Myers-Briggs (MBTI)**
March 15: **Writing Effective E-mail Messages**
March 24: **Getting Things Done Across Organizational Borders** **[more]**

April 13: **Designs for the High-Speed, Broadband Information Age** **[more]**

Feb 23: **Silicon Valley Engineers Week Banquet**

Reception – Dinner – DiscoverE Presentation – Awards
SVEC Engineering Hall of Fame Induction Ceremony for
Dr. Douglas Engelbart, Inventor of computer Mouse and a recipient of National Medal of Technology
Kenneth Levy, Founder and COB of KLA-Tencor Corp, Academy of Engineering
Dr. Dan Maydan, President Emeritus of Applied Materials, Academy of Engineering
Dr. David Patterson, Chair of EE and Computer Science, UC Berkeley, Academy of Engineering
Dr. T.J. Rogers, Founder, President and CEO, Cypress Semiconductor **[more]**

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February *2005 • Volume 52 • Number 2*

IEEE **GRID** is the monthly newsmagazine of the San Francisco Bay Area Council of the Institute of Electrical and Electronics Engineers, Inc. As a medium for both news and opinion, the editorial objectives of IEEE **GRID** are to inform readers in a timely and objective manner of newsworthy IEEE activities taking place in and around the Bay Area; to publish the official calendar of events; to report on IEEE activities of a national and international scope; and to serve as a forum for comment on areas of concern to the engineering community by publishing contributed articles, invited editorials and letters to the editor.

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From the editor . . .

After the roads had been cleared from the mid-January snowstorms, I headed over to Bishop, CA to have some fun in the snow (and to babysit some grandkids). As we drove down 395 and approached Mono Lake, the sight we saw is shown in the cover photo this month. I've never seen Mono Lake covered with this sort of fog before. The cold air (about -10°C or 15°F) and the relatively warm lake water sets up a freezing fog that blankets the basin for days at a time and deposits hoarfrost on all the trees, bushes, and grass – really ethereal. The mountain to the left is Boundary Peak (dividing Nevada and California), with Mount Montgomery to the right. Farther right is White Mountain (in Nevada), with the Mono Craters poking out of the fog.

Every engineer would like lifetime employability. This will usually mean bridging two or three careers, with substantial retraining or on-the-job learning. It also seems to require some amount of networking – being in contact with your peers, learning and sharing, and knowing (when the time comes) who can give you some assistance. Review some of the technical and professional development classes listed on Page 1, to see if some of these skills might not make you more productive – and more employable. Then, come see what the experts say, at the PACE meeting on February 22nd. I'll see you there!

Paul Wesling **editor@e-grid.net**

NOTE: This PDF version of the IEEE GRID – the **GRID.pdf** – is a monthly publication and is issued a few days before the first of the month. It is not updated after that. Please refer to the Online edition and Interactive Calendar for the latest information: **www.e-GRID.net**

Professional Services Marketplace – editor@e-GRID.net for information

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Silicon Valley Engineers Week Banquet 2005

Wednesday, February 23, 2005

Westin Hotel, Great America Parkway (two blocks from US 101)

Agenda

5:30 PM	Reception and No-Host Bar
6:30 PM	Welcome by SVEC President
6:45 PM	Dinner with Friends
7:15 PM	Recognition of Sponsors and Distinguished Guests
7:30 PM	Discover-E Presentation
7:40 PM	15th Anniversary Review
8:10 PM	SVEC Engineering Hall of Fame Induction Ceremony
9: 00 PM	Scholarships
9:15 PM	Close

Hall of Fame Inductees

Dr. Douglas Engelbart, Inventor of computer "Mouse" and a recipient of National Medal of Technology

Kenneth Levy, Founder and COB of KLA-Tencor Corp, Academy of Engineering

Dr. Dan Maydan, President Emeritus of Applied Materials, Academy of Engineering

Dr. David Patterson, Chair of EE and Computer Science, UCB, Academy of Engineering

Dr. T.J. Rogers, Founder, President and CEO Cypress Semiconductor

"The Alliance for Engineering Leaders in Silicon Valley"

Silicon Valley Engineering Council is dedicated, through a network of volunteers and local engineering societies, to meeting the needs of the engineers of today and of tomorrow.

AFE	***ECSCV***
AIAA	***IEEE***
AIChE	*NSPE*
AISES	***O/E#130***
ASCE	***SAMPE***
ASMI	***SFPE***
ASME	SME
CETA	SPE
CSPE	***SWE***

Visit our web page at **www.svec.org**

We appreciate the Silicon Valley / San Jose Business Journal's participation in SVEC engineering activities.

Companies are encouraged to sponsor Engineers Week 2005

- **Engineer's Week Corporate Sponsor** ($20,000) includes four student scholarships and special project support
- **Platinum Sponsor** ($15,000) includes two student scholarships and special project support
- **Gold Sponsor** ($10,000) includes two student scholarships
- **Silver Sponsor** ($5,000) includes one student scholarship

For further sponsorship and banquet information call Jay Pinson, (408) 997.9857, email: pinsonjay@aol.com

Tear here

2005 Engineers Week Banquet Reservation Form

$70.00 per person until 2/04/2005 … $80.00 after 2/04/2005 Number of Attendees _____ Total Amount

Name: _____

Company/Society: _____

Address: _____

_____

City, State, Zip: _____

Phone: _____

Email: _____

Send Reservation forms and checks to: **Silicon Valley Engineering Council**
P.O. Box 611865
San Jose CA 95161

Questions? Email: engelhardte@asme.org Phone: (408)565-9978 (Russ Yarp)

Dinner includes salad of Wild And Baby Field greens with Mustard Vinaigrette. Also Chocolate Cup Filled with Mousse and Seasonal Berries.

__ Chicken Florentine –Spinach, Swiss Cheese and Garlic Herb Boursin Cheese Sauce
__ Pacific Salmon Filet – Lemon Peppered, Saffron Sun Dried Tomato Dill Sauce
__ Broiled Filet Mignon with Brandy Flambeed Wild Mushrooms
__ Baked Vegetable Wellington – Spinach, Vegetables, Wild Rice, and Gouda Cheese Wrapped in Puff Pastry, Wild Mushroom Sauce

_____ **Total Number of Dinners**

Please include all names of attendees so name badges & seating can be prepared in advance.

Make checks payable to: **Silicon Valley Engineering Council**

Credit Card reservations and more information available at **www.svec.org/banquet**

IEEE Professional Skills Courses

new! **Communication & Conflict Management using Myers-Briggs (MBTI)**

Date/Time: Tuesday, March 8, 8:30 AM – 4:30 PM
Instructor Linda Price
Location: Carl Zeiss Meditec, Dublin

The Myers-Briggs Type Inventory (MBTI) is the most widely used instrument in the world to gain a deeper understanding of self, others and interpersonal relationships. It provides insights on the four basic "people patterns" that hold the key to leadership styles, effective communication, conflict, team building and productivity.

Key Topics: - Discover your Myers-Briggs Type Indicator - Gain insights into your own strengths and blindspots - Understand four basic "people patterns" and how they think and act - Learn how to not interpret others' differences and value diversity - Discover your preferred communication and conflict style - Build trust and rapport through communication - Practice how to communicate and influence each type - Recognize barriers to effective communication - Listen for problem statement, content and intention - Learn how to use questions that gain quality information - Separate facts from emotions - Speak with clarity and commitment - Use a model to work through and resolve conflict

new!

Writing Effective E-mail Messages

Date/Time: Tuesday, March 15, 8:30AM-4:30PM
Instructor: Kathleen Mohn
Location: Synopsis Corp, Sunnyvale

A step-by-step process for designing and writing clear business emails. The training involves writing, revising, and editing exercises; critiquing documents; games; and lecture. You will walk away with confidence in writing and editing skills and a consciousness about international writing.

Engineering Management & Components, Packaging and Manufacturing Technology Societies, SCV Chapters

Getting Things Done Across Organizational Borders

Date/Time: Thursday, March 24, 8:30AM-4:30PM
Instructor: Dr. Andrew Oravets
Location: Synopsis Corp, Sunnyvale

"Right-sizing" and restructuring have put new emphasis on lateral communication and inter-departmental cooperation. This seminar introduces you to innovative practices for dealing with people who do not report to you-but whose assistance and support are critical. You will be provided with new perspectives on the root causes of your communication blockages with others, as well as, practical techniques for assessing the styles of others, uncovering their needs and reaching mutually satisfying agreements.

Key Topics: - Learn strategies for creating results with people within or outside your direct control - Obtain "mind share" from people who have other priorities - Develop techniques for reaching people who are "impossible to deal with" - Evaluate the strengths and weaknesses of your favorite "fix-it formula" for solving issues with others - Demonstrate style flexibility to get a better hearing - Explore alternative ways to describe projects and proposals - Learn new negotiation tools to bargain for results across organizational boundaries - Employ practical techniques for making clear, concise requests - Reach mutually satisfying agreements

Improve your skills – register for one of these classes. Bring a team!

For complete information and registration form, see our Chapter website, right-hand column:

www.cpmt.org/scv/

SSR2005: March 9-11, 2005, San Francisco

The 2nd International Symposium on Systems and Human Science

Engineered Complex Systems in the 21st Century

*-Examining the multi-disciplinary dependencies in maintaining **Safety, Security** and **Reliability***

Convenient access and parking -- Westin Hotel SF Airport, in Milbrae

SSR2005

Topics include:

- Integration of Systems and Human Sciences
- Methodology/Concepts/Tools
- Robotics
- Risk Management/Decision Analysis
- Complexity, Uncertainty and Non-Linearity
- Networks/Sensors/Communications
- Data Fusion

- **Facilitating the development of new ideas and approaches for the 21st Century**
- **Supporting the creation and evaluation of engineered complex systems**
- **Building reliable capabilities for large scale disasters**
- **Integrating disciplines to provide solutions for the future**

Papers accepted through Feb 2005

Visit the website @ http://ssr.llnl.gov

Co-sponsored by:

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Technical Co-Sponsor: IEEE Systems, Man, and Cybernetics Society

For more information, contact
Sandra Maldonado, Conference Coordinator
Phone 925-423-0621
ssr@llnl.gov

IEEE Professional Skills Courses

Engineering Management & Components, Packaging and Manufacturing Technology Societies, SCV Chapters

Presentation Skills for Engineers

Date/Time: Friday, February 18, 8:30AM-4:30PM
Instructor: Peter Rosselli
Location: Verisign Corp., Mountain View

This program is for professionals who are called upon to make formal or informal presentations – to deliver their ideas clearly, demonstrate confidence and enthusiasm, and handle objections with poise. Class size is limited to 10 participants.

Key Topics: - - Conquer "stage fright" - Use effective eye contact & gestures - Optimize opening & closing statements - Make key information memorable - Create & use visual aids - Use notes skillfully - Handle challenging questions & difficult people

new!

Writing Effective E-mail Messages

Date/Time: Thursday, February 24, 8:30AM-4:30PM
Instructor: Kathleen Mohn
Location: Exar Corp., Fremont

A step-by-step process for designing and writing clear business emails. The training involves writing, revising, and editing exercises; critiquing documents; games; and lecture. You will walk away with confidence in writing and editing skills and a consciousness about international writing.

Clear Business and Technical Writing

Date/Time: Tuesday, February 15, 8:30AM-4:30PM
Instructor: Kathleen Mohn
Location: Carl Zeiss Meditec, Dublin

Key Topics: Planning a Business/Technical Document - Formatting Information According to Purpose - Organizing for Readability - Wording Title & Headlines - Writing Your Content Using Plain English - Avoiding Ambiguity & Vagueness - Revising for Style - Trimming the Fat - Editing for Correct Grammar Usage - Activating Active Voice - Editing for Appropriate Punctuation Usage - Writing Typical Technical Reports - Writing Clear Processes and Procedures - Handling International Writing

Improve your skills – register for one of these classes. Bring a team!

For complete information and registration form, see our Chapter website, right-hand column:

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The Largest System Design Event in North America

EMBEDDED SYSTEMS CONFERENCE

March 6 – 10, 2005
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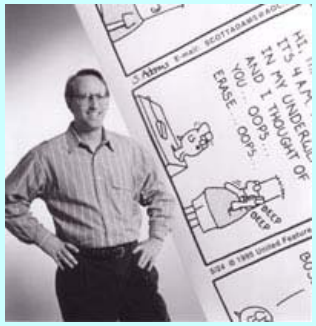
Visit www.esconline.com/sf/ CLICK!

The Embedded Systems Conference offers an exciting line-up of special events. All of our special events are free to registered attendees and range from keynote addresses to networking opportunities and receptions, to panel discussions all designed to enrich your event experience.



Keynote Address:
Cartoonist Scott Adams:
From Cubicles to Comics
Tues March 8, noon - 1:00 PM

Design Seminar Keynote:
Software Defined Radio — Business, Market, and Social Ramifications
Stephen M. Blust and Mark Cummings, SDR Forum
Wed March 9, 2-3 PM

Panel Discussions

The Future of Processors for Signal Processing Applications
Monday, March 7; 6–7 PM

After the Storm: How the Industry has Changed Forever
Wednesday, March 9; 1 – 2 PM

Engineering Humanity: Managing the Chaos
Thursday, March 10; 10:00am - 11:00am

Plus Other Panel Discussions:
- Moving Beyond 3G: Where Do We Go From Here?
- The Transformation of the TV
- Silicon Support at Layer 7: XML, SOAP, and Vertical Protocols
- The Future of Wireless Networking

Technical Program

Sunday full-day tutorials

• User Interface Design • Migrating from a Legacy RTOS to Embedded Linux • Scaling System Design • Embedded Linux Jumpstart • Embedded C Programming • Introduction to Real-Time Operating Systems • Real-Time UML

Monday full-day tutorials

• Real-Time Kernels • System Architecting and Tradeoffs • Managing Embedded Projects • Real-Time Design Guidelines and Rules of Thumb • Embedded GNU Jumpstart • Crafting Embedded Systems in C++ • Architectural Design of Device Drivers • TCP/IP Networking

$645 for one full day; $995 for BOTH days

Plus 132 three-hour and 90-minute Technical Classes on Tuesday through Friday– see the Advance Program for listing/descriptions and times for each topic.

Register now to ensure your participation!

www.esconline.com/sf/program

Seven full- or multi-day DESIGN SEMINARS:

- **Analog and Power** (Monday – 2 tracks)
- **DSP Performance** (Monday – 2 tracks)
- **Easy Paths to Silicon** (Mon & Tues, 2 tracks)
- **Consumer Systems** (Tues & Wed, 2 tracks)
- **3G Cellular Systems** (Tues & Wed, 2 tracks)
- **Wireless Networking** (Wed & Thurs, 2 tracks)
- **Network Systems** (Wed & Thurs, 2 tracks)

... and the new
Microprocessor Summit (Monday) – new-product introductions in AM; three tracks on shipping products in PM

Visit the Exhibits *(free admission)*

The Embedded Systems exhibits floor features leading companies showcasing cutting-edge hardware, software, tools, and the full spectrum of system components! You will learn relevant new skills, meet and talk with vendors, network with peers, and develop new strategic partnerships – all under one roof, at one time, with both daytime and evening hours:

Tues 1-8pm – Wed 10am-7pm – Thurs 9am-2pm

Visit www.esconline.com/sf/exhibits CLICK!

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Register by February 8th for early-bird rates!

Visit www.esconline.com/sf/ for full details

Ride BART or MUNI to the Powell Street station

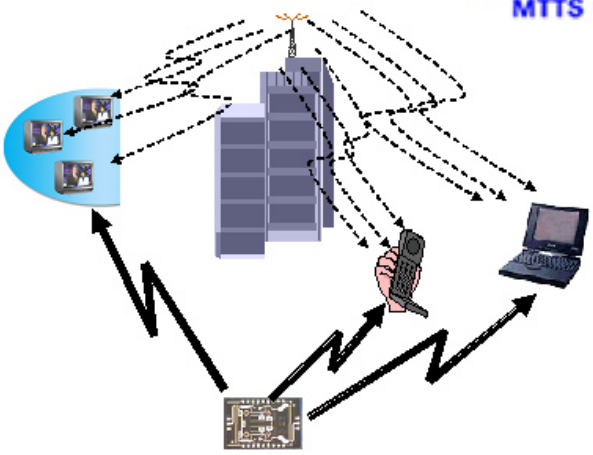
Annual Half-day Workshop:

Designs for the High-Speed, Broadband Information Age

- **Wednesday, April 13, 2005**
- **Seminar: 8:30 AM – Noon**
- **Registration/Breakfast: 8 AM – 8:30 AM**
- **Santa Clara Convention Center**
- **In conjunction with IEEE WESCON'05**
- **Includes free admission to WESCON exhibits**
- **Plenty of free parking**

Microwave Theory & Techniques Society
Santa Clara Valley Chapter

MTTS ®



Design the Future!

As the need for higher data rates and faster user interfaces increases, demands are placed on both the technology used to transmit and receive this information and on its designs. Previously, the realm of high speed, high frequency, high bandwidth circuits was relegated to III-IV materials like GaAs or InP. Recently, advances in materials like Si and SiGe have forced designers to look at these technologies to keep the cost low and to be competitive. Additionally, innovations like those in newer materials like GaN have been sought to provide advantages for these types of circuits.

Therefore, the ability to understand how the requirement for higher speed and faster data rates drives microwave circuit designs and the ability to design circuits in these various technology choices is an important part of the contemporary engineer's job as well as his/her value to an organization. The main challenges for today's microwave circuit designer are to understand which technology to use for a given application and know the tradeoffs and limits when designing in these technologies.

This seminar will explore the advances that have been made in these various material technologies and their affect on IC designs. Speakers will cover:

- The applications and requirements for higher speed and faster data rates
- The advantages and disadvantages of these technologies for handling higher speed/data rate applications
- How the need for faster and increased quantity of information affects circuit designs
- Current examples of designs and the tradeoffs addressed

Registration is through the
SF Bay Area Council Office:
Marilyn Turner Phone 650-327-6622
345 Forest Avenue
Palo Alto, CA 94301

PROGRAM

100GHz CMOS Circuits and the High Speed Broadband Information Age
Dr. Luiz Franca-Neto, Technical Leader and Manager, Broadband Wireless Division (BWD) Intel Communications Group (ICG), Intel Corporation

SiGe and RFCMOS Technology for the High Speed Information Age
Dr. Xiaojuen (Ben) Yuan, Ph.D, IEEE Senior Member, Vice Chair, SSC/AP/MTT IEEE San Diego Chapter, IBM West Coast Foundry Applications

InP HBT Design for 100 to 200GHz IC's
Dr. Zachary Griffiths, Post Doc Researcher, UC Santa Barbara

SiC and GaN Based Transistor and Circuit Advances
Mr Simon Wood Principal RF Design Engineer, Cree Microwave

REGISTER TODAY!

Space is limited, so please mail in your registration by April 6. Registration fee includes breakfast and the course CD (proceedings).

Registration Fee:	Pre-Reg'n by Apr 9	After Apr 9.
IEEE Members	$50	$65
Nonmembers	$75	$90
Student/Retired	$30	$30
Unemployed *	$30	$30

* Bring or send a photocopy of unemployment check receipt dated within 2 weeks of registration to qualify

For Workshop registration information, please visit the MTT Chapter website:

www.mtt-scv.org

Microlithography 2005

The International Society for Optical Engineering

27 February – 4 March 2005
San Jose Convention Center
www.spie.org/events/ml05
Conferences – Courses – Exhibits

Six Conference Tracks:

Emerging Lithographic Technologies
EUV Systems/Optics/Materials - Advanced Mask Characterization – Nanoimprint - Maskless Lithography - Electron Projection Lithography - Novel Lithography Systems

Metrology, Inspection, and Process Control
OPC/RET - Overlay, Registration Errors - SEM/Scatterometry for Critical Dimension Metrology - CD Measurement and Reference Systems/Comparisons - Overlay Tool and Mark Development - Line Edge Roughness - Integrated Metrology/Design - Line Edge Slimming - Mask-Related Defect Analysis - CD Uniformity Control

Advances in Resist Technology & Processing
Immersion - 193nm/157nm Materials - ARC/Bilayer - EUV/E-beam - Novel Materials/Applications/Processing - Pattern Collapse/Defectivity - Resist Processing – Simulation - Line-Edge Roughness - ARC/EUV

Optical Microlithography
Polarization and High NA - Immersion Lithography - Low K1 Process Control & Performance - Image Quality & Characterization - Image and Process Modeling - Mask Polarization Effects - Advanced Lithographic Materials - Advanced Exposure Systems and Components

Data Analysis & Modeling for Process Control
Advanced Process Control - Data Modeling for Control - CD Uniformity Control - Advanced Process Control - Methods for Data Analysis and Automation

Design and Process Integration for Microelectronics Manufacturing
Design, Automation and Characterization - Design Optimization and RET - Analysis and Modeling - Design for Yield - OPC and RET

Plenary Presentations: (full details in Advance Program)

Full-chip CD analysis and design optimization for 90-nm node and below, Christopher Spence, AMD

The flat panel display paradigm: Successful implementation of Microelectronic Processes on Gigantic Wafers, Zvi Yaniv, CEO, Applied Nanotech

Lithographic Technologies that Haven't (yet) Made it: Lessons Learned, Fabian Pease, Stanford U.

Panel Discussions:
Can NGL Crest the 32nm Summit: Where is the window of opportunity for emerging lithography? • Seamless integration of metrology and design for development and validation of OPC and RET • DfM Innovation Sources: Venture-backed companies, public corporations and academia

Short Courses (Separate registration allowed)

Take advantage of these courses and workshops taught by leaders in the field – bring yourself up-to-date on the hottest technologies or get the background basics you need. You can register for Short Courses without attending the full Symposium.

Sunday full-day courses

Intro to Microlithography: Theory, Materials, & Processing • 193-nm Lithography • Lithography Control and Characterization • Lithographic Optimization: A Theoretical Approach

Sunday half-day courses

Introduction to Electron-Beam Lithography • Basics of Optical Imaging in Microlithography: Hands-on • Nano-Scale Patterning with Imprint Lithography • Instruments and Methodologies for Accurate Metrology • Pushing the Limits: Optical Enhancement, Polarization, and Immersion Lithography • 157-nm DUV Lithography • Optical Lithography Modeling • Intellectual Assets for Micro/Nanolithography

Full-day courses during the week

Applying Optical Proximity Correction and DfM • Plasma Etching and Reactive Ion Etching • Resists for Deep UV Lithography • Data Management: Understanding Chip-finishing, Tapeout, and Data Preparation

Plus 13 others – see the Advance Program for listing/descriptions

Course capacity is limited -- register now to ensure your participation!

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6th International Symposium on

QUALITY ELECTRONIC DESIGN

March 21-23, 2005
DoubleTree Hotel, San Jose

www.isqed.org

ISQED is the leading international conference dealing with design for manufacturability and quality issues front-to-back. The conference spans three days, Monday through Wednesday, in three parallel tracks, hosting nearly 100 technical presentations, six keynote speakers, two panel discussions, workshops/tutorials and other informal meetings. ISQED proceedings are published by IEEE Computer Society and hosted in the digital library. Proceedings CD ROMs are published by ACM.

Technical Sponsorship by IEEE Components, Packaging & Manufacturing Technology Society (CPMT), IEEE Electron Devices Society (EDS)
In cooperation with
IEEE Circuits and Systems Society (CASS)
ACM Special Interest Group on Design Automation (ACM/sigDA)
Fabless Semiconductor Association (FSA).

CONFERENCE HIGHLIGHTS

TUTORIALS/WORKSHOPS

ISQED 2005 offers a single full-day tutorial track focusing on a range of critical issues in circuit design and packaging at sub-90nm CMOS. We are pleased to have five noted experts in their respective fields (Design methodologies for implementing Robust Circuits with desired Power Performance Characteristics, Managing Leakage Power, Circuit Design in the Presence of Uncertainty, and Modeling and Design of Chip-Package Interface) to present the latest research in these compelling areas as follows:

Design of sub-90nm Circuits and Design Methodologies
Ruchir Puri, IBM TJ Watson Research Center, NY
Sachin Sapatnaker, Electrical & Computer Engineering, University of Minnesota
Tanay Karnik, Intel Circuit Research Labs, Hillsboro, OR
Rajiv Joshi, IBM T J Watson Research Center, NY

Modeling and Design of Chip-Package Interface
Luca Daniel, Massachusetts Institute of Technology, Cambridge, MA
Byron Krauter, IBM Microelectronics, Austin, TX
Lei He, UCLA EE Dept, Los Angeles, CA

PLENARY SESSIONS

Two plenary sessions will be held on Tuesday and Wednesday mornings. Six industry & academia leaders will discuss the issues surrounding manufacturability and electronic design from various points of view. Plenary keynote speakers are:
John Kibarian, President & CEO, PDF Solutions
Ashok K. Sinha, Sr. VP & GM, Applied Materials
Joe Sawicki, Vice President & General Manager, Mentor Graphics
Aki Fujimura, Chief Technology Officer, Cadence Design Systems
Kurt A. Wolf, Director, Library Management Division, TSMC
Bernard Candaele, Department Head, SoC, IC & EDA, Thales, Paris, France

TECHNICAL SESSIONS

ISQED Technical sessions start on Tuesday March 23 and continue until the afternoon of Wednesday March 24. Besides the above plenary sessions, panel discussions, and workshops, the program consists of seventeen technical sessions, featuring up to 80 papers on various challenging topics related to design for manufacturability and quality. A list of topics includes:

- Tools, Flows & IP Blocks: Interoperability and Implications (EDA)
- Design for Manufacturability & Quality (DFMQ)
- Design Verification and Design for Testability (DVFT)
- Package-IC Design Interactions and Co-Design (PDI)
- Robust Device, Interconnect, and Circuits (RDIC)
- Physical Design, Methodologies and Tools (PDM)
- Effects of Technology on IC Design, Performance,Reliability, Yield (TRD)
- System Level Design, Methodologies and Tools (SDM)

Please refer to the ISQED web site at **www.isqed.org** for information regarding the tutorials, conference, and hotel registration. Direct all conference inquiries to **isqed@isqed.org**. Early registration is recommended to take advantage of the discounted registration fee.

PANEL DISCUSSIONS

ISQED is pleased to offer two high-power evening panel discussion sessions, where many leading experts, address the important issue of quality design. These panels would focus on the following topics:
1. **IP Creation and Use**
   What roadblocks are ahead or it is just a clear and bumpy road?
2. **Nanoelectronics: Evolution or Revolution?**

LUNCHEON SPEECH

IP Quality: A Design, not a Verification Problem
Michael Keating, Synopsys

See the full Advance Program and Tutorial Descriptions (21 pages, 225kB PDF):

Download Now

Visit the ISQED website for more information and to register:

www.isqed.org

Early Registration through March 14th – save $100

SCV Lasers and ElectroOptics

TUESDAY February 1

Cavity Enhanced Spectroscopy

Speaker: Dr. Barbara Paldus, CTO, Picarro
Time: Networking and Pizza Social at 7:00 PM; Presentation at 8:00 PM
Place: National Semiconductor Credit Union Auditorium, 955 Kifer Rd., Sunnyvale
RSVP: please email to aaronhaws1000@yahoo.com
Web: www.ieee.org/scv/leos

Barbara Paldus is the CTO at Picarro and is responsible for technology strategy, research innovation, and business development. She leads the team that develops the company's breakthrough photonic technology. She has 14 awarded patents, 13 pending patent applications, and has published over 30 journal and conference papers, as well as two book chapters, on cavity ring-down spectroscopy (CRDS) and lasers. She has been recognized with 12 research and academic awards, most recently the Adolph Lomb Prize (2001) by the OSA. Barb received both her Ph.D. and M.S.E.E. degrees from Stanford University. She received her BS in electrical engineering and applied mathematics from the University of Waterloo, Canada.

This review will address state-of-the-air cavity enhanced spectroscopies, specifically cavity ring-down spectroscopy (CRDS). CRDS can provide high sensitivity, high precision, and absolute calibration in a wide range of environments. The talk will report on a compact cavity ring-down spectrometer that can be applied in a wide variety of applications. The ring-down spectrometer is fully contained in two 5 ¼" tall, 19" wide rack mount enclosures and utilizes a robust, near-infrared, fiber-coupled tunable diode laser. The instrument has a baseline noise level of 8×10^{-11} cm/Hz$^{1/2}$. Specific applications that will be illustrated will include measurement of trace ammonia in air, trace atmospheric toxic industrial compounds such as hydrides (Arsine/Silane), and the isotopic composition of biological molecules such as carbon dioxide and water. The talk will also present results on CRDS instrument performance, including zero drift, precision, absolute accuracy, and linearity over a wide range of environmental operation conditions. Finally, extensions of CRDS technology to media other than gases will be presented. Recent results with liquid media will be presented.

SCV Electromagnetic Compatibility

TUESDAY February 8

Locating ESD and other Impulsive Events by Time of Arrival

Speaker: Douglas C. Smith, IEEE Senior Member, EMC Society Board of Directors
Time: Social 5:30 PM; Presentation 7:00 PM
Place: Applied Materials Bowers Cafeteria, 3090 Bowers Ave., Santa Clara
RSVP: not required
Web: www.scvemc.org

Now that fast digital scopes are widely available, it is now practical to locate impulsive events using a few simple handmade antennas and looking at time delays of the wavefront. Examples will be discussed and a live demonstration given.

Douglas C. Smith held an FCC First Class Radiotelephone license by age 16 and a General Class amateur radio license at age 12. He received a BS-EE degree from Vanderbilt University in 1969 and an MS-EE degree from the California Institute of Technology in 1970. In 1970, he joined AT&T Bell Laboratories as a Member of Technical Staff. He retired in 1996 as a Distinguished Member of Technical Staff. Recently, he was Manager of EMC Development and Test at Auspex Systems in Santa Clara, CA and is now an independent consultant. Mr. Smith is a Senior Member of the IEEE and a member of the IEEE EMC Society Board of Directors.

His technical interests include high frequency effects in electronic circuit design, including topics such as signal integrity, design reliability, Electromagnetic Compatibility (EMC), Electrostatic Discharge (ESD), Electrical Fast Transients (EFT), and other forms of pulsed electromagnetic interference. He also has been involved with FCC Part 68 testing and design, telephone system analog and digital design, IC design, and computer simulation of circuits. He has been granted over 15 patents, several on measurement apparatus.

Mr. Smith has lectured at Oxford University, the University of California at Berkeley, Vanderbilt University, AT&T Bell Labs, and at many public and private seminars on high frequency circuit design, troubleshooting, measurements, ESD, and EMC. He is author of the book High Frequency Measurements and Noise in Electronic Circuits. He maintains a practical engineering website at **www.dsmith.org** containing nearly 100 useful technical articles.

SCV Electron Devices

TUESDAY February 8

Optoelectronics at Work: from Optical Inverters to Detectors

Speaker: Dr. Rebecca Welty, Lawrence Livermore National Laboratory
Time: 6:00 PM (pizza & soda, no cost), 6:15 PM Presentation
Place: National Semiconductor Credit Union, Bldg. 31, 955 Kifer Rd., Sunnyvale
RSVP: not required
Web: www.ewh.ieee.org/r6/scv/eds/announcements/ieee-scv-eds-20050201.html

Rebecca J. Welty received the B.S. degree in Electrical Engineering from the University of California at Davis in 1997. In 1999 she received the M.S. degree and in 2002 the PhD degree in Electrical Engineering, from the University of California at San Diego. In 2002 she joined Lawrence Livermore National Laboratory.

Photonic integrated circuits require the ability to integrate both lasers and waveguides with low absorption and coupling loss. This technology is being developed at LLNL for digital logic gates for optical key generation circuits to facilitate secure communications. Our overall PIC circuitry is based on the gain lever and quenching phenomena. This talk highlights the device development which has been done. We demonstrate an approach of integrating InGaAs DQW edge emitting lasers with electron beam evaporated dielectric waveguides to form low loss optical interconnects.

The second part of this talk is on new materials and devices for radiation detection. We are investigating the use of semiconductor-based nanomaterial elements as an electrical signal generation media for the detection of neutrons. The main advantage of detectors made of these new materials over standard neutron semiconductor detectors is that the high neutron cross-section converter materials can be embedded in the semiconductor detector elements rather just coated on the surface of the detectors as in the case for the conventional neutron semiconductor detectors.

SCV Communications

WEDNESDAY February 9

Open Wireless Architecture (OWA) for Next Generation Wireless and Mobile Communications

Speaker: Prof. Willie W. Lu, Stanford University.
Time: 6:00 p.m. (pizza & soda),
6:30 p.m. presentation
Cost: $1 donation to partially cover food cost
Place: National Semiconductor Credit Union, Bldg. 31, 955 Kifer Rd., Sunnyvale
RSVP(required): rsvp@comsocscv.org
Web: www.comsocscv.org

Willie W. Lu is a consulting professor at Stanford University, and a special advisor on emerging technologies and strategies to several China information and communications authorities including the Ministry of Information Industry. Prof. Lu was a member of the Technological Advisory Council of the U.S. Federal Communications Commission and a senior principal architect and vice president of Siemens and Infineon Technologies. He is also an internationally recognized senior expert in emerging wireless technologies and has been a senior technical advisor for 22 wireless communication authorities in more than 10 countries. He has guest edited about 50 special issues on emerging wireless communications in IEEE, IEICE, ACM, CIC and other major publications, and has had over 150 papers published in major professional publications. Prof. Lu is a member of the editorial board of IEEE **Spectrum** and has been technical chairman of numerous IEEE conferences including GLOBECOM'03, WCNC'02, and VTC'03, and wireless feature editor of IEEE **Communications** Magazine, IEEE **Transactions on Wireless Communications** (former J-SAC Wireless), and others. He is a frequent keynote and featured speaker at technical fora, and a prominent wireless pioneer on the worldwide basis. He is a member of IEEE, ACM, IEICE, CIC, CIE and Sigma Xi. Willie is also the founding chairman of the prestigious World Wireless Congress, Global Mobile Congress and Fourth Generation Mobile Forum (4GMF), and has been a distinguished Chinese wireless expert overseas by various Chinese authorities since 1996.

User expectations for wireless mobile communications are increasing with regard to a large variety of services and applications with different degrees of quality of service (QoS) related to delay, data rate and bit error requirements. Therefore, seamless service and applications via different access systems and technologies that maximize the use of available spectrum will be the driving forces for future developments.

Given the increasing demand for flexibility and individuality in society, the mean for the end-user might be assessed. Potentially, the value would be in the diversity of mobile applications, hidden from the complexity of the underlying communications schemes. This complexity would be absorbed into an intelligent personality management mechanism, which would learn and understand the needs of the user and control the behavior of their reconfigurable and open wireless terminals accordingly in terms of application behavior and access to support services.

This vision from the user perspective can be implemented by integration of these different evolving and emerging wireless access technologies in a common flexible and expandable platform to provide a multiplicity of possibilities for current and future services and applications to users in a single terminal. Systems of 4G mobile will mainly be characterized by a horizontal communication model, where different access technologies such as cellular, cordless, WLAN type systems, short range wireless connectivity and wired systems will be combined on a common platform to complement each other in an optimum way for different service requirements and radio environments – technically called "Converged Broadband Wireless Platform", or "Open Wireless Architecture" (OWA).

OWA will eventually become the global solution, integrating various wireless air-interfaces into one wireless open terminal where the same end equipment can flexibly work in the wireless access domain as well as in mobile cellular networks.

Based on the "Mission 2020 Plan in Wireless and Mobile Communications" in many countries, including the European Union and China, OWA has become the No.1 focused subject of research, development and strategy in the industry.

WEDNESDAY February 9

From Printed Circuit Boards to Substrates: Reflecting on the History of these Technologies

Speaker: Bernd Appelt, Director of ASE Materials Substrate Marketing, ASE Europe
Time: Seated dinner at 6:30 ($25 if reserved before Feb 6; $30 after & at door; vegetarian available); Presentation at 7:30 PM
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Via PayPal on website, or email to Janis Karklins
Web: www.cpmt.org/scv/

Bernd Appelt received his PhD in polymer science at the University Of Mainz, Germany. Subsequently he post-doced at the University of Massachusetts with Roger Porter and at IBM Research with Gus Ouano. He spent many years in IBM Endicott, New York, in various R&D and M.E. positions before joining ASE as Director of Marketing for ASE Materials Substrates.

His work has focused on packaging technologies, developing new materials and processes for printed circuit boards as well as substrates, implementation of water-based process technologies and establishing Teflon-based substrate technologies. He also managed the PWB licensing program within IBM. Bernd has published numerous technical papers and holds many patents.

Organic substrate technology is the basic building block for almost all PBGA packages today. How did this technology get started? And what are the future challenges? Organic substrates are essentially small printed circuit boards and have extensively replaced ceramic substrates as chip carriers. The predominant substrate is the plastic ball grid array (PBGA) substrate which was conceived out of the need for surface mountable substrates with a vision for lower substrate cost and better electrical performance. The lower cost advantage over ceramic was based on the form factor used to manufacture printed circuit boards, and its mature industry.

This presentation will outline some of the history in development of PBGA substrates and the corresponding manufacturing challenges that had to be overcome. Lastly, some of the current development needs, also driven by environmental demands, will be highlighted.

Engineering Management & Components, Packaging and Manufacturing Technology Societies, SCV Chapters

Getting Things Done Across Organizational Borders

Date/Time: Thursday, March 24, 8:30AM-4:30PM
Instructor: Dr. Andrew Oravets
Location: Synopsis Corp, Sunnyvale

"Right-sizing" and restructuring have put new emphasis on lateral communication and inter-departmental cooperation. This seminar introduces you to innovative practices for dealing with people who do not report to you-but whose assistance and support are critical. You will be provided with new perspectives on the root causes of your communication blockages with others, as well as, practical techniques for assessing the styles of others, uncovering their needs and reaching mutually satisfying agreements.

Improve your skills – register today.
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For complete information and registration form, see our Chapter website, right-hand column:

www.cpmt.org/scv/

SCV Computer & Stanford Student Branch

THURSDAY February 10

A RISKS-Oriented View of Software Development

Speaker: Peter G. Neumann, Principal Scientist, Computer Science Lab, SRI International
Time: 7:00 PM - Refreshments, 7:30 PM - Technical Presentation
Place: Room 380C, Stanford Univ Main Quad, (free parking after 6 PM; from Palm Drive oval enter the last door on the right of the main building and take the elevator down - follow signs from there)
RSVP: not required
Web: www.siliconvalleycs.org/

Peter G. Neumann (Neumann@CSL.sri.com) has doctorates from Harvard and Darmstadt. After 10 years at Bell Labs in Murray Hill, New Jersey, in the 1960s, during which he was heavily involved in the Multics development jointly with MIT and Honeywell, he has been in SRI's Computer Science Lab since September 1971. He is concerned with computer systems and networks, security, reliability, survivability, safety, and many risks-related issues such as voting-system integrity, crypto policy, social implications, and human needs including privacy. His book, **Computer-Related Risks**, has gone through five printings, and is now being cranked out as needed by Addison-Wesley. He is on the Editorial Board of IEEE Security and Privacy. He moderates the ACM Risks Forum, edits CACM's monthly *Inside Risks* column, chairs the ACM Committee on Computers and Public Policy, and co-founded People For Internet Responsibility (PFIR). He is a Fellow of the IEEE, ACM, and AAAS, and is also an SRI Fellow. He is the 2002 recipient of the National Computer System Security Award. He is a member of the U.S. Government Accountability Office (formerly General Accounting Office) Executive Council on Information Management and Technology, and the California Office of Privacy Protection advisory council. He has taught at Stanford, U.C. Berkeley, and the University of Maryland. See his Web site for further background, Senate and House testimonies, bibliography, etc.

Henry Petroski long ago noted that we learn very little from our successes (of which there are relatively few in large software projects) and that we need to learn much more from our failures (which are numerous in computer systems). With respect to software development, there are many lessons we should be learning from many cases collected in the Online Risks Forum and the ACM SIGSOFT Software Engineering Notes. Based on these cases, this talk will consider some of the main challenges in developing trustworthy systems and networks that must (for example) be secure, reliable, and survivable in the face of a wide range of adversities. This is not simply a turn-the-crank process, and requires great ingenuity, experience, discipline, and above all, managerial understanding and control. The difficulties of realistically applying the engineering aspects of what is euphemistically called software engineering are enormous; significant discipline is required that is seldom found in practice, in addition to inherently robust architectural concepts that allow facile composition of systems and networks out of subsystems. For example, we need more efforts such as those suggested half a century ago by Shannon and von Neumann in building trustworthy systems out of less trustworthy components. Furthermore, vision is needed to avoid excessive costs and delays in development and serious risks in operation; to manage development efforts; to inspire relevant long-term research; to anticipate and minimize problems of usability; and above all, to enable the creation of effective long-term strategies and to recognize that short-term strategies are often counterproductive technologically.

The talk will be illustrated with numerous examples from the RISKS archives. Extensive background can be found at:

- Neumann's home page www.csl.sri.com/neumann
- Principled Assuredly Trustworthy Composable Architectures:
  www.csl.sri.com/neumann/chats4.ps
  www.csl.sri.com/neumann/chats4.pdf
  www.csl.sri.com/neumann/chats4.html
-The ACM Risks Forum

SCV Microwave Theory and Techniques

THURSDAY February 10

High Frequency Vector Network Analyzer Calibration Basics

Speaker: Ken Wong, Agilent Technologies, Inc.
Time: 6:00 PM - Refreshments and Social Hour, 7 PM - Technical Presentation
Place: Agilent Technologies, Santa Cruz conference room, Bldg 50, 5301 Stevens Creek Blvd, Santa Clara
RSVP: not required
Web: www.mtt-scv.org/

The Vector Network Analyzer (VNA) is one of the essential instruments for high frequency device and system designers for product testing. It is a very complex instrument. Its measurement accuracy depends on the calibration method and calibration standards used. This presentation will cover the basic theory of VNA, VNA calibration, calibration standards and models and accuracy factors.

Ken Wong has been with the Hewlett-Packard Company and now Agilent Technologies for over thirty years. His experience at HP/Agilent includes product design, manufacturing process development, and test process development of microwave hybrid microcircuits and instruments. Currently, he is a senior engineer responsible for the development, design, modeling, and measurement of precision microwave electronic and mechanical calibration and verification standards and calibration methodology of Vector Network Analyzers. He has published and presented many papers on VNA calibration and standards. He has served as the Vice-President, President and the current Treasurer of ARFTG (Automatic Radio Frequency Techniques Group). He is a senior member of the IEEE, a member of MTT-12 technical committee and the IMS2006 Steering Committee. He is also a member of Tau Beta Pi, and Eta Kappa Nu

Annual Half-day MTT Chapter Workshop:

Designs for the High-Speed, Broadband Information Age

- **Wednesday, April 13, 2005**
- **Seminar: 8:30 AM – Noon**
- **Registration/Breakfast: 8 AM – 8:30 AM**
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SCV Magnetics

TUESDAY February 15

Spin Torque, and Nanorings

Speaker: Prof. C. L. Chien, 2005 IEEE Magnetics Society Distinguished Lecturer & Department of Physics & Astronomy, Johns Hopkins University
Time: Coffee and conversation at 7:30 PM, Presentation at 8:00
Place: Komag, 1710 Automation Pkwy, San Jose
RSVP: not required
Web: www.e-grid.net/docs/0502-scv-mag.pdf

Chia-Ling Chien received the B. S. degree in Physics from Tunghai University in Taiwan in 1965, and Ph. D. degree in Physics from Carnegie-Mellon University in 1972. He has been a faculty member in the Department of Physics and Astronomy at Johns Hopkins University since 1976, where he is the Jacob L. Hain Professor in Arts and Sciences. He currently directs the Material Research Science and Engineering Center on Nanostructured Materials at Johns Hopkins. His recent research focuses on magnetic nanostructures including magnetic granular solids, nanowires, multilayers, and arrays of rings and dots, and the exploration of GMR, exchange bias, half-metals, spin torque effects, Andreev reflection, and point-contact spectroscopy. He has written more than 330 journal articles and holds several patents. He is one of the ISI 1120 most cited physicists. He has served as Meeting Chair and Chair of the Advisory Committee of the Conference on Magnetism and Magnetic Materials. He has been awarded honorary professorships at Nanjing, Lanzhou, and Fudan universities in China. He has been a Fellow and the 2004 recipient of the David Adler Award of the American Physical Society.

The exploration of magnetic nanostructures in recent years has resulted in a string of discoveries such as interlayer coupling, giant magnetoresistance (GMR), exchange bias, and tunneling magnetoresistance. Some of these effects were utilized as read-heads in high-density magnetic recording and non-volatile magnetic storage only a few years after the original discovery. In this talk, I will describe two new topics in magnetic nanostructures from inception to realization to potential applications.

Since electrons have spin in addition to charge, a spin-polarized current carries angular momentum. For a large current density, the angular momentum can exert a substantial torque onto a receiving magnetic entity to excite spin waves or even to switch its magnetization. The spin torque effects are accomplished in the absence of an external magnetic field. The salient aspects of the spin torque effects in different contexts, such as switching and magnetic recording without a magnetic field, will be described.

Nanorings are small entities with special attributes of several magnetic states with unique switching characteristics. A magnetic nanoring can also support vortex state despite its very small size. The two chiralities of the vortex state can be exploited for magnetic recording purposes. Multilayered nanorings have also been proposed as vertical random access memory (VRAM) units. However, fabrication of nanorings using e-beam lithography has considerable limitations in the number of rings, ring size, and areal density. We have developed a new method with which a large number (109) of small (100 nm) rings can be fabricated with an areal density of 45 rings/μm^2. The magnetic and other characteristics of such arrays of nanorings will be described.

WEDNESDAY February 16

On-demand Technology Development for Medical Imaging Clinical Trials

Speaker: Vivek Swarnakar, Vice President of Engineering, Synarc, Inc.
Time: Dinner with the speaker in the Stanford Hospital cafeteria at 6:15 PM (No reservation needed); Presentation at 7:30 PM
Place: Room M114 in the Stanford Hospital (see website for map)
RSVP: not required
Web: www.ieee.org/scv/embs/pages/upcoming.html

Vivek Swarnakar is the Vice President of Engineering at Synarc, where he is responsible for managing a team of about 60 engineers located in the USA and Europe and engaged in developing technology used to support clinical trials. Dr. Swarnakar has a Ph.D from the State University of New York at Buffalo, a Masters degree from the Rochester Institute of Technology and a Bachelor's degree from the Universidade Federal da Paraiba, Campina Grande in Brazil, all in Electrical Engineering. He has published numerous peer-reviewed articles in the medical imaging area covering radiation-oncology, medical image compression, telemedicine and computer-aided detection (CAD). Dr. Swarnakar has over 20 years of software development experience in research and industrial settings. For the last 10 he has applied imaging technology and engineering principles to the medical field including work on a radiation therapy planning system, a digital mammography system and a computer aided breast cancer detection system. His research interests include fractals, neural networks, image analysis and compression. He has been an IEEE member for over 11 years.

Synarc is the world's largest central radiology service dedicated to clinical trials. Synarc provides services that integrate all aspects of the design and execution of clinical trials that use imaging and molecular markers across a spectrum of therapeutic areas including Arthritis, Cardiovascular, Neurology, Oncology, Orthopedics and Osteoporosis. Managing a clinical trial requires having the ability to efficiently and reliably support data collection, quality assurance, analysis, storage and retrieval. This is a multi-disciplinary effort that by design requires close collaboration of several business entities, hospitals and medical imaging sites. The requirements for implementing technical solutions for this industry are quite complex and often result in a development model that can be described as "on demand technology development". The on-demand aspect is driven by logistics and human processes natural to this industry. These include clinical trial end-point definition, ability to recruit patients for a clinical trial as well as monitoring safety of drugs. All development efforts have to be carried out in a manner where strict adherence to applicable regulatory guidelines is maintained at all times. In his talk, Dr Swarnakar, who heads the Engineering department at Synarc, will discuss typical challenges commonly encountered in developing technology for managing imaging based clinical trials on a global scale.

THURSDAY February 17

Electromagnetic Interference Shielding for New Communication Products

Speaker: Dr. Rocky Arnold, Chief Technical Officer, WaveZero
Time: 6:30 - 7:00 PM Pizza;
7:00 - 8:30 PM Presentation
Place: Bishop Ranch 1, 6101 Bollinger Canyon Rd, San Ramon, CA (just off I-680) - see website for map
RSVP: Please send a quick note to oeb@comsoc.org to allow us to order the correct number of pizzas, by Feb. 16
Web: www.comsoc.org/oeb/

. **Dr. Rocky Arnold** is a co-founder of WaveZero and served as its CEO from 2000-2004. Rocky has over 20 years of experience involving research, the creation of intellectual property, and the commercialization of technology. In the 10 years prior to founding WaveZero, Rocky working with emerging high technology companies and their entrepreneurial leaders to develop start-up strategies and business plans for securing initial rounds of funding. Rocky has M.S. and Ph.D. degrees in Engineering from Stanford University, an M.S. degree in Mechanical Engineering from MIT, a B.S.M.E. degree from the University of Missouri, and an MBA from Notre Dame De Namur University. Rocky served in the U.S. Army and U.S. Army Reserves to the rank of Captain with distinction.

Combating electromagnetic interference is one of the most important design objectives for communications equipment designers. Newly introduced methods and products solve these problems while at the same time comply with new mandated regulations. Performance characteristics and benefits of new shielding products will be discussed.

The European Union (EU) has approved two directives that directly affect global OEMs and their new product introduction (NPI) teams. The first is called WEEE standing for Waste Electrical and Electronic Communications Equipment and requires "producers" of electronic communications equipment for distribution in the EU to provide for recovery and recycling of their electronic products. The second directive, Restriction on Hazardous Substances or RoHS affects which materials are used in the construction of an electronic device and notably eliminates lead from current lead-based solders. These regulations in concert with new regulations for electromagnetic compliance (EMC) now strongly drive the choice of materials, components, and processes made by NPI teams. This talk will briefly review the WEEE and RoHS Directives and discuss how these new regulations affect new product design of communications equipment especially in regards to the choice of EMI shielding. We will contrast older methods of shielding (metal cans and conductive paint on plastic) with a new EMI shielding material based on the thin film metallization of thermoformed structure.

We will continue our feature at the meeting of providing some networking time for those who want to stand and make a brief announcement. If you're looking for a new position, have a position to fill, want to let us know that your new start-up is ready for business or have a similar announcement, bring your resumes, job descriptions or company brochures and be prepared to make a match. Please keep your statements brief, so we'll have time for everyone. There will be time before and after the formal meeting for one-on-one discussions.

OEB Industry Appplications

THURSDAY February 17

Short Circuit and Coordination Analysis Studies

Speaker:	Glyn J. Lewis , P.E., Applied Power Co.
Time:	No-host social at 5:30 PM, Presentation at 6:15PM, Dinner at 7:15PM, Presentation continues at 8:00PM
Place:	Marie Callender's Restaurant - The Garden Room, 2090 Diamond Blvd, Concord (near Concord Hilton Hotel). Call 925-827-4930 for directions
Cost:	Dinner is $22 for IEEE members, $25 for non-members.
RSVP:	Please make reservations by Feb 16 by contacting Gregg Boltz, gboltz@brwncald.com, or call (925) 210-2571.
Web:	www.ewh.ieee.org/r6/oeb/ias.html

The speaker will be **Glyn J. Lewis**, P.E., who is a consulting electrical engineer with the firm Applied Power. Mr. Lewis has a 40 year career in the electrical industry. He graduated from the University of Wales Institute of Science and Technology in 1964 and worked for two switchgear suppliers in the UK as a commissioning engineer.

Mr. Lewis joined General Electric Company in 1968 and worked in a number of positions until forming his own company Applied Power in 1981. He is a member of IEEE, NFPA, NETA, IAEI and ASE and he is a registered P.E. in the State of California.

Glyn has performed over 400 analytical studies on electrical distribution systems in the areas of short circuit analysis, coordination, load flow and motor starting. He has been responsible for the design of numerous generating and cogenerating plants. He has served as the principal instructor for many training seminars presented by General Electric Company in the fields of electrical safety, switchgear and protective relaying.

On the local IEEE level, Glyn was selected as an instructor in the San Francisco short course on high voltage substation design. He was also selected by IEEE as an instructor in 1984, 1985, 1987, 1991, 1993 and 1994 to conduct the San Francisco and Los Angeles Industrial Application Society's and the Power Engineering Society's short courses on fault calculations and coordination studies.

Producing electrical short circuit and coordination studies today is now more of a science than an art as in years gone by. The new science is by virtue of the plethora of computer programs now available at comparatively low cost for use by electrical engineers. These software tools are created by people who have rigorously studied the multitude of electrical standards and incorporated the methodology into their programs. However, we are still left with the longstanding problem of interpreting the final results. Usually this requires further knowledge of the specific hardware devices and their application standards.

This month's meeting will offer some helpful guidelines and advice from an industry veteran on producing and then analyzing the computed and graphical results of electrical system studies. The presentation marks a return to the basics for our IEEE chapter and will be educational for both younger engineers as well as seasoned veterans. All interested parties are welcome to attend.

SCV Solid State Circuits

THURSDAY FEBRUARY 17

SiGe Heterojunction Bipolar Technology and Applications

Speaker: Jayasimha Prasad, Maxim Integrated Products
Time: Refreshments at 6:30 PM (donation requested to partially cover food cost); presentation at 7:00 PM
Place: Cadence Building 5, 2655 Seely Ave, San Jose (map on website)
RSVP: by email to ssc_scv_rsvp@yahoogroups.com or call 408 894-2646.
Web: www.ewh.ieee.org/r6/scv/ssc/

Jayasimha Prasad obtained his Ph.D in Electrical Engineering from Oregon State University, Corvallis. For the past twenty years he has been engaged in developing high-speed GaAs and SiGe HBT technology. He was with Tektronix for 12 years developing GaAs-based HBT technology for high-speed oscilloscopes. As a Tektronix Fellow, he was the first in the world to demonstrate a 60GHz InGaP HBT IC technology with 28ps gate delay. During the past 9 years, he has been with National Semiconductor, Micrel Semiconductor and new Maxim Integrated Products where he has developed SiGe BiCMOS processes for wireless and fiber optic applications which have resulted in several products. Prior to the HBT work, Prasad developed E^2PROM processes at National Semiconductor and contributed to VMOS processes at AMI Semiconductor. Prasad is a Distinguished Lecturer for the IEEE Electron Devices Society. He is a member of the IEEE technical committees on Compound Semiconductor Devices, Compact Modeling, and Education. He is also a member of the IEEE Technical Field Awards Committee. Prasad has served on the technical program committees for BCTM and IEDM.

In the past two decades, there has been a phenomenal growth in Silicon-Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) technology. The devices have migrated from a mere laboratory curiosity to full-fledged manufacturing of highly dense integrated circuits. More and more commercial HBT circuits are being introduced into the market almost every day. The unity-gain cutoff frequency (f_T) and the maximum oscillation frequency (f_{max}) have reached record highs. SiGe HBTs have demonstrated f_T and f_{max} of 350GHz and 340GHz respectively. Current Mode Logic (CML) ring oscillator gate delays have hit a low of 3.3ps. What makes this technology even more interesting is that the HBT can be easily integrated into a standard CMOS flow, yielding a highly functional SiGe BiCMOS process capable of realizing analog, digital, RF and microwave circuits. These have become mainstream processes throughout the industry and they are also being offered by the well-known semiconductor foundries.

SiGe HBTs have found a presence in the least expensive consumer products, such as cell phones, to the most expensive gigabit communications systems. The improved performance of the devices has resulted in impressive circuit results. Dynamic frequency dividers operating at 110GHz and oscillators running at 98GHz have been reported. SiGe power amplifiers with an output power of 220 watts and power-added efficiency of 46% have been demonstrated. In high-speed communication circuits, 50Gb/s 4:1 MUX/DMUX, and 43Gb/s Clock and Data Recovery (CDR) have been shown with SiGe HBTs. This talk will focus on the physics, status of the technology, applications and future prospects of SiGe HBT technology.

SCV Consultants' Network of Silicon Valley

TUESDAY February 22

High Tech Recovery! Is it going to be as good as it has been?

Speakers: Art Rahman and Carl Angotti
Time: Networking 7:00 to 7:30 PM; Presentation at 7:30
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), S'vale (**Note**: this is a new meeting place)
RSVP: none needed
Web: www.ieee-sv-consult.org/

Art Rahman (IEEE Senior Member, and the recipient of Professional Achievement Award in 1999) is the founder of IEEE CNSV, and served for three years at the National Alliance of IEEE Consultants' Networks Coordinating Committee (AICNCC). He has been a speaker at National Conferences throughout the country. He presented a Paper as an invited speaker at the Hong Kong Productivity Council in 1996. Mr. Rahman holds a BSEE, and did graduate work at Santa Clara Univ. He has worked in the high tech industry for over 25 years in the management, design & development of very successful projects. As an independent consultant for twelve years (dba: Info Science), he has provided services in the area of I/O subsystem design and development, and he is an expert witness in patent litigations. He has actively traded equities and options for the last five years.

Carl Angotti has been an Electronic Engineering Consultant for more than 25 years, so he has been through many of the Valley's ups and downs. He is a Senior Member of PATCA (Professional and Technical Consultants Assoc.), a member and past Chair of the IEEE Consultants Network of Silicon Valley and a past Chair of the IEEE Engineering Management Society of Santa Clara Valley. Mr. Angotti holds an MSEE from the University of Southern California, a BSEE from Carnegie-Mellon University and an MBA from San Jose State University. He has spoken several times at the Consultants' Network. His company, Angotti Product Development, (www.angotti.com) provides consulting services in systems and circuit design, and project management focused on new product development to a wide variety of companies in the Bay Area.

This will be an interactive meeting that is intended for self-employed and independent consultants.

First, Art Rahman will present new data he has gathered on the state and health of the US high technology industry.

Then, Carl Angotti will share some of his views on the current economic health of Silicon Valley. Using his expertise in consulting business management, he will give some ideas on how we can face the new challenges heading our way. Some independent consultants have diversified their businesses either in the same industrial sector, or in a completely new venture, while others are still waiting for the economy to turn around.

After this, the floor will be opened up for questions and comments from those attending the meeting. During this meeting, you can listen, then judge for yourself where the industry is going in the next 12 months. Join with our speakers and your fellow consultants for this informative and provocative meeting.

SCV Product Safety Engineering

TUESDAY February 22

Effective Environmental Stress Screening, and Lab Tour

Speaker: Dr. Hong S. Liu, President, Quanta Labs
Time: 6:00 to 6:45 PM - free pizza & sodas; 6:45 - 7:45 - Program; 7:45 - 8:30 - Tour
Cost: no admission charge
Place: Quanta Laboratories, 3199 De La Cruz Blvd., Santa Clara
RSVP: Limited number for tour - you must RSVP to geldridge@apple.com
Web: www.e-grid.net/docs/0502-scv-pses.pdf

Environmental Stress Screening (ESS) is a powerful tool to precipitate weaknesses in product design, components, and manufacturing processes. ESS (sometimes called HALT and HASS) can help companies limit the risk of product recall, meet government/commercial requirements to ruggedize their products and reduce the chance of safety defects. This presentation will describe the ESS process and how to effectively apply it to your products.

Interested members of other local IEEE Society Chapters are encouraged to attend!

For a map to the location, please visit www.quantalabs.com and click **Contact Us.**

Speaker (and Tour Guide): **Dr. Hong S. Liu**

Dr. Liu is the founder (in 1985) and president of Quanta Laboratories. He received his Ph.D. in Mechanical Engineering from the University of California at Berkeley, and MS in Mechanical Engineering from the University of Washington. Dr. Liu has over 30 years experience in environmental testing, as well as extensive experience in research, development and testing of mechanical and electronic devices, and theoretical and experimental stress analysis. He is a writer/contributor to **Test Magazine** and has developed 3 patents in environmental testing. Dr. Liu also has taught engineering courses at the University of California at Berkeley and engineering and business courses at San Jose State University.

SCV PACE - Professional Activities Committee for Engineers

TUESDAY February 22

The Realities and Myths of Engineer Retraining

Speakers: Panel of industry and education professionals
Time: Dinner (optional) at 6 PM; Panel/Discussion (no charge) 7 PM
Cost: $15 non-member/$10 member for dinner
Place: Cadence, Building 5, 2655 Seely Ave, San Jose
RSVP: To reserve your dinner, email Jonathan David (j.david@ieee.org) and pay at the door
Web: www.ewh.ieee.org/r6/scv/scv_pace.html

Worker retraining has been the mantra for generations of displaced engineers who find their skills outdated or insufficient for a changing workplace. But what does retraining really mean? How do you navigate through the plethora of training and educational opportunities as you transition back into a productive work environment? If I take this class or complete this certification, will they come?

These and many other questions will be addressed at the next IEEE-PACE forum on Engineering Retraining. This event, cosponsored by CSIX Connect (www.csix.org), offers a carefully chosen panel of industry and education professionals presenting their views in a moderated discussion relevant to working engineers as well as engineers in career transition. Because of the changing work environment, keeping current on many career topics is just as relevant to the engineer as is the latest technical advance.

Attendees should expect to take away a better sense of evaluating the various training and retraining options available to them, insights into the minds of those making the hiring decision and the relevance and importance of the human touch - networking - in their career growth and satisfaction.

If you are a working engineer concerned that you might be impacted by a layoff, or if you have been laid off and are considering retraining, this event is a must.

IEEE Professional Skills Courses

SCV Chapters, Engineering Management & Components, Packaging and Manufacturing Technology Societies

Presentation Skills for Engineers

Date/Time: Friday, February 18, 8:30AM-4:30PM
Instructor: Peter Rosselli
Location: Verisign Corp., Mountain View

Key Topics: - - Conquer "stage fright" - Use effective eye contact & gestures - Optimize opening & closing statements - Make key information memorable - Create & use visual aids - Use notes skillfully - Handle challenging questions & difficult people

new!

Writing Effective E-mail Messages

Date/Time: Thursday, February 24, 8:30AM-4:30PM
Instructor: Kathleen Mohn
Location: Exar Corp., Fremont

A step-by-step process for designing and writing clear business emails. The training involves writing, revising, and editing exercises; critiquing documents; games; and lecture. You will walk away with confidence in writing and editing skills and a consciousness about international writing.

Clear Business and Technical Writing

Date/Time: Tuesday, February 15, 8:30AM-4:30PM
Instructor: Kathleen Mohn
Location: Carl Zeiss Meditec, Dublin

Key Topics: Planning a Business/Technical Document - Formatting Information According to Purpose - Organizing for Readability - Wording Title & Headlines - Writing Your Content Using Plain English - Avoiding Ambiguity & Vagueness - Revising for Style - Trimming the Fat - Editing for Correct Grammar Usage - Activating Active Voice - Editing for Appropriate Punctuation Usage - Writing Typical Technical Reports - Writing Clear Processes and Procedures - Handling International Writing

For complete information and registration form, see our Chapter website, right-hand column:

www.cpmt.org/scv

SCV Components, Packaging & Manufacturing Technology

THURSDAY February 24

High Frequency Fullwave Simulation of Packages

Speaker: Dr. An-Yu Kuo, Optimal Corp.
Time: buffet lunch at 11:45 AM ($15 if reserved before Feb 21; $20 after & at door; vegetarian available)
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: to John Jackson, Analog Devices, at john.jackson@analog.com
Web & Map: www.cpmt.org/scv

Dr. An-Yu Kuo, Chief Technical Officer, co-founded Optimal Corp. in 1995. Previously, he was Associate at Structural Integrity Associates, where he was responsible for sales and consulting projects. Dr. Kuo has won several grants from the U.S. government, and developed a breakthrough full-wave field solver that is many times faster than the competitors' products. Dr. Kuo received his BSME from National Tsing-Hua University, MSME from National Taiwan University, and Ph.D. in Theoretical and Applied Mechanics from University of Illinois.

SCV Monterey Bay Subsection

SATURDAY February 26

Radiofest - Public Service Event for Demonstrating Science and Technology for the Public Welfare

Event: free - includes many 1-hour talks, plus demonstrations of radio modes, and a vendor fleamarket
Time: 7:00 AM - 2 PM
Place: General Stilwell Community Center, on old Fort Ord, in Marina
RSVP: none required
Web & Map: www.radiofest.org/

Co-sponsored with the Naval Postgraduate School Amateur Radio Club, this free event includes many 1-hour talks, plus demonstrations of various amateur radio modes, and a vendor fleamarket at the Stillwell Community Center on old Fort Ord.

Examples of some of the talks are:

- Homeland Security - How it affects you.
- Be Prepared! Assemble your Emergency Preparedness Kit
- How to become a licensed Ham in 2 hours
- IRLP: Internet Radio Link Program, Worldwide Communications
- Tools for Teachers: Science, Math & Engineering Aids
- Achieving Success using Amateur Satellites
- Using 802.xx products in the Amateur bands
- A joint Amateur/CSU Monterey Bay wireless network initiative
- Automatic Antenna Tuners for Portable Operation
- Winlink on the Central Coast Community Emergency Response Teams (CERT) in Monterey County

WEDNESDAY March 16

New, Ultrahigh-Thermal-Conductivity Materials

Speaker: Dr. Carl Zweben
Time: Seated dinner at 6:30 ($25 if reserved before Mar 13; $30 after & at door; vegetarian available); Presentation at 7:30 PM
Place: Ramada Inn, 1217 Wildwood Ave (Fwy 101 frontage road, between Lawrence Expy and Great America Pkwy), Sunnyvale
RSVP: Via PayPal on website, or email to Janis Karklins at karklins@ieee.org
Web: www.cpmt.org/scv/

Dr. Carl Zweben, an independent consultant, has directed development and application of advanced packaging materials for over 30 years, and was the first to use Al/SiC. For many years, he was Advanced Technology Manager and Division Fellow at GE Astro Space. Other affiliations have included DuPont, Jet Propulsion Laboratory and the Georgia Institute of Technology NSF Packaging Research Center. Dr. Zweben was the first, and one of only two winners of both the GE One-in-a-Thousand and Engineer-of-the-Year awards. He is a Fellow of ASME, ASM and SAMPE, an Associate Fellow of AIAA, and has been a Distinguished Lecturer for AIAA and ASME. He has published and lectured widely on advanced thermal management and packaging materials.

In the last two years, there have been revolutionary advances in thermal management materials. There are now 16 low-CTE (coefficient of thermal expansion) materials with thermal conductivities between that of copper (400 w/m-K) and 4X copper (1600 W/m-K). Some are low cost. Others have low-cost potential in high-volumes. Most have low densities. They have a wide range of electrical properties that can minimize electromagnetic emissions or provide EMI shielding. Several are now in production applications, including servers, plasma displays, laptops, and printed circuit boards, marking historic packaging milestones. For comparison, traditional low-CTE materials like copper/tungsten have thermal conductivities that are little or no better than that of aluminum (200 W/m-K). Payoffs include: improved thermal performance, reliability, alignment and manufacturing yield; reduced thermal stresses, simplified thermal design; direct solder attach, elimination of liquid cooling, fans and heat pipes; weight savings up to 85%; size reductions up to 65%; and lower cost. This talk discusses the large and increasing number of advanced composite and monolithic materials, including properties, manufacturing processes, development status, applications, and future directions, including nanocomposites.

CONFERENCE CALENDAR

The **CONFERENCE CALENDAR** is a service to our IEEE Members. It outlines upcoming IEEE workshops and conferences in the Bay Area. Please submit items to the GRID Editor: editor@e-grid.net.

Conferences are also encouraged to purchase display space in the **GRID.pdf** and publicize their events on our website and in our **e-GRID** email notification service. For the Conference Publicity flyer, please download:

www.e-grid.net/docs/conf-flyer.pdf

February 27 – March 4: **Microlithography Symposium this year in San Jose**

SPIE's Microlithography Symposium brings practitioners of micro- and nano-lithography together in an exciting, informative, and interactive environment. It includes six Conferences tracks, 30 courses, and 130 exhibits.

Hear the latest about state-of-the-art applications and techniques, as well as emerging issues as you are presented with new challenges and alternative technologies. This variety in topic becomes all the more important as optical lithography, historically the dominant patterning technology, faces tough challenges in providing the patterning solutions for leading edge semiconductor manufacturing. Microlith'05 is held at the San Jose Convention Center.

For full information, please visit the website:

www.spie.org/events/ml05

and **see Page 9**

March 6-10: **Embedded Systems Conference in San Francisco at Moscone Center**

The Embedded Systems Conference offers an exciting line-up of special events, 132 technical classes, 16 full day tutorials, 6 Design Seminars and over 350 exhibits. The Microprocessor Summit is a forum for major semiconductor companies to talk about their near-future plans and make new-product announcements. All of the special events are free to registered attendees and range from keynote addresses to networking opportunities and receptions, to panel discussions all designed to enrich your event experience. Discounts for teams registering together; free admission to the Exhibits. For more information:

www.e-grid.net/conf/embed05.html

and see Page 7

March 9-11: **International Symposium on Systems and Human Science – Safety, Security, Reliability comes to Milbrae**

SSR2005 is intended to facilitate the development of new ideas and approaches for the 21st Century to support the creation and evaluation of engineered complex systems -- consisting of machine, software, and human elements -- on which our modern societies increasingly depend for safety, security, and well being. Papers are still being accepted, and the Advance Program can soon be downloaded (email Sandra at **ssr@llnl.gov**). See:

ssr.llnl.gov and **Page 6**

March 13-17: **Semiconductor Thermal Measurement, Modeling, and Management (SEMI-THERM) Symposium at the Fairmont Hotel in San Jose**

SEMI-THERM is an international forum dedicated to the thermal design and characterization of electronic components and systems, and this year it's in the SF Bay Area. Technical sessions cover Air, Liquid, and System-level Cooling, Thermal Interface Materials, Performance and Reliability, Nanoscale/Microscale Thermal Solutions, Stacked Die, and Thermal Characterization. The two-day short course is "Thermal Design Fundamentals- From Air to Liquid Cooling" with Dr. Kaveh Azar.. The Advance Program can now be downloaded:

www.semi-therm.org

March 21-23: **International Symposium on Quality Electronic Design at DoubleTree in San Jose**

With the theme "Design for Quality in the Era of Uncertainty," ISQED is the pioneer and leading conference dealing with design for manufacturability and quality issues, front to back. It spans three days, Monday through Wednesday, in three parallel tracks, hosting nearly 100 technical presentations, six keynote speakers, two panel discussions, workshops/tutorials and other informal meetings. The Advance Program can now be downloaded:

www.isqed.org and **See Page 10**